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13. ABSTRACT *(Maximum 200 words)*

The objective of this work was to show proof of concept for a writable RFID tag that used an integrated antenna and MRAM nonvolatile memory to store data. Circuit designs for the reader/writer unit and the the tag IC were completed during the work, and showed that the design concept was feasible. MRAM memory cells specifically designed for this low energy application were constructed and tested, and are clearly suitable for use in this application. These memory cells offer bipolar signals for easier sensing during the read cycle, and are denser than the ROMs normally used in read-only RFID tags, leading to a lower IC cost. Four different integrated antennas, using two IC processes developed specifically for this work, were constructed during the course of the program. The processes were developed to be used on top of existing circuitry, so the antennas would pose no area penalty on the IC. Problems with the new processes prevented successful fabrication of any of the antenna designs; however, extensive failure analysis was performed on the completed parts, and the processing problems have been conclusively identified. Good parts are expected with a mask modification and several minor process modifications. NVE considers the program a major success, and will submit a Phase II proposal.

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Low Cost Writable RFID Tag with MRAM Memory

ARPA SBIR Program #DAAH04-94-C-0032

Final Report
March 1, 1995

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Table of Contents

Introduction

This report summarizes the results of this Phase I program. The program objectives, as stated in the Phase I proposal, were as follows:

1. Design and fabricate a high quality inductor using NVE's plated permalloy process, for use as an on-chip antenna.
2. Design the analog power supply circuitry required to interface the previously fabricated coil with CMOS or BiCMOS circuitry.
3. Design a low power MRAM memory cell for use in an RFID application. Fabricate and test an array of these memory cells.
4. Design the circuitry required for a 128 bit array of these MRAM memory cells.
5. Design the system circuitry for a remote RF Reader/Writer. This portion of the work was subcontracted to WJ Systems, Inc.

This report is composed of four sections that individually address the five work objectives listed above(the two circuit oriented objectives are combined in one section). Here is a brief overview of the results and conclusions from this work:

Objective 1 was expanded at the beginning of Phase I to include design and test of four different types of inductors, not just two. Because of the extensive process development required, this objective proved to be much more difficult than anticipated; nevertheless, significant progress was made during Phase I, and NVE is confident that this objective can be successfully completed during Phase II.

Objectives 2 through 5 were successfully completed during the course of the program. The work conclusively showed that using MRAM memory cells was feasible on an RFID chip, and that the circuits required to drive them are able to be constructed using standard CMOS or BiCMOS technology. Also, integration of a write cycle into the system architecture was proved feasible by WJ Systems.

NVE draws the following conclusions from this Phase I effort:

- The integrated antenna processing has been debugged, and initial processing runs during the next phase of the program have a 90% or better chance of resulting in working parts.
- An MRAM memory cell has been developed which meets the requirements for a writable RFID application.

- The on-chip circuitry required for integrating the antenna and the MRAM memory cells into a functional RFID chip has been almost completely defined, and no barriers to production of a commercial part have been found.
- Designing and building the system circuitry for the reader/writer is straightforward, and does not form a barrier to commercialization
- NVE is very pleased with the outcome of this work, and will propose a Phase II effort that will result in a prototype RFID system based on the results of the Phase I effort.

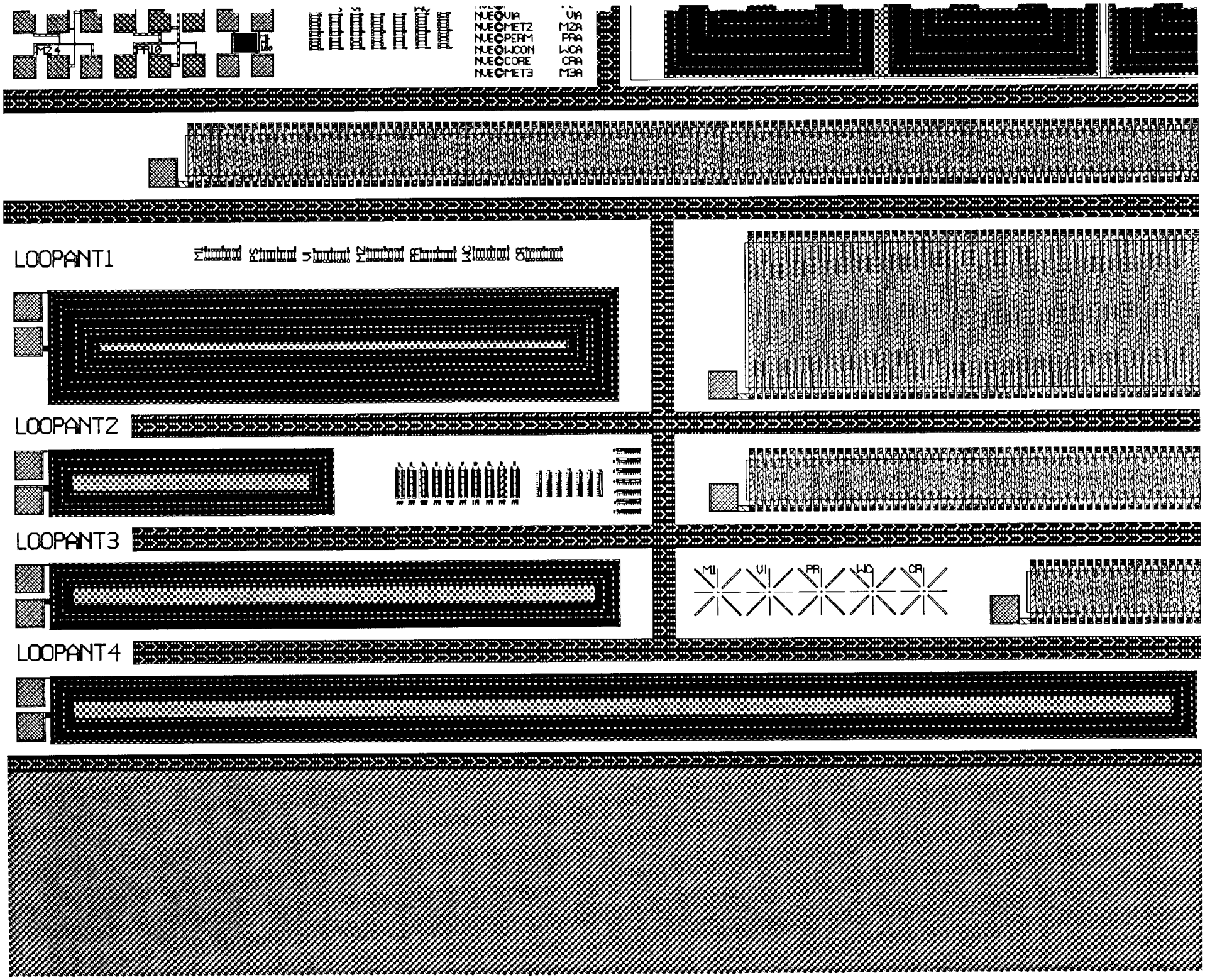
On-Chip Inductor Development

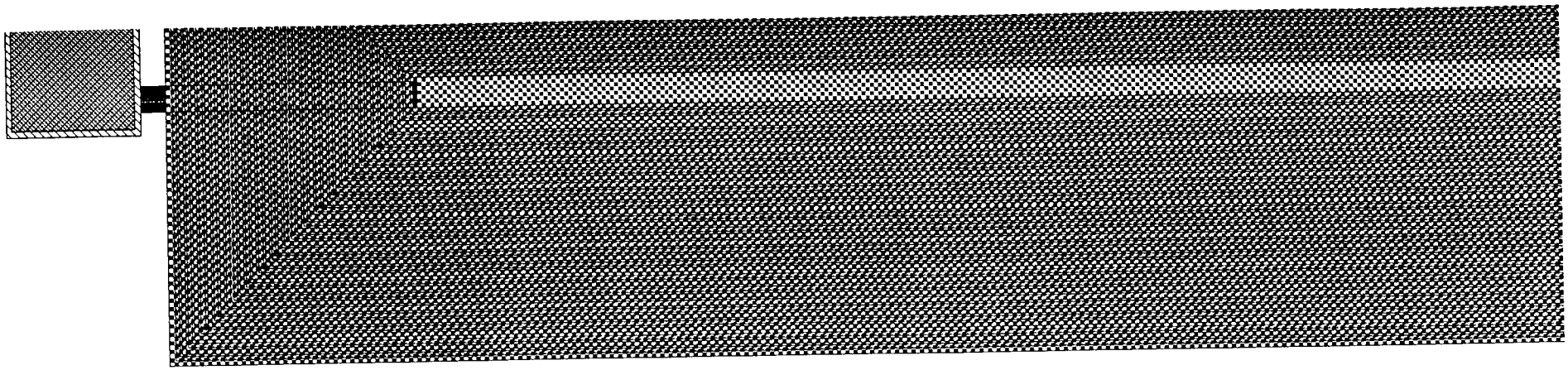
Originally in the Phase I proposal, NVE had proposed development of two types of integrated inductors that could be used as an antenna for an RFID chip. Between the time when the Phase I proposal was submitted and the Phase I work actually began, NVE came up with several more promising designs for an integrated antenna. During the first month of the program, these designs were investigated in detail, and the two most promising designs were included in the mask set along with the original two designs. The four separate designs are described individually below. A brief description is given of each design, along with plots and photomicrographs of the actual device. A table provides the silicon area each design occupies and its nominal resistance. A description of the process required to manufacture the inductor is given, and the results of the frequency response tests conducted at the end of the program are provided. Conclusions are drawn at the end of each section regarding the merit of each design. The names of the designs were selected more or less arbitrarily.

1. LOOPANT - This integrated inductor was one that was described in the Phase I proposal. It uses NVE's standard permalloy plating process, and is the only inductor manufactured during this program to do so. Because it used a standard process, this inductor was also the only one that went through processing without problems.

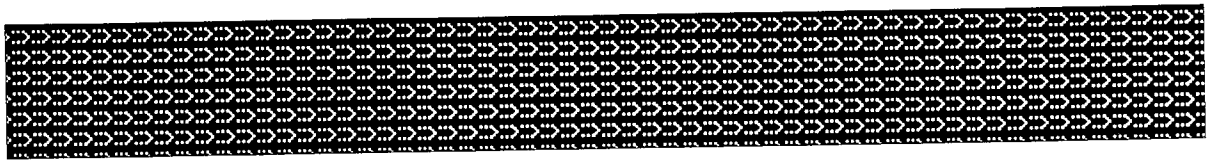
This design is essentially a coil of semiconductor metal(98% Al, 2% Cu) underneath a thick plated permalloy shield. The function of the permalloy shield is to increase the self inductance of the coil. The high self inductance would provide a high voltage at the terminal connections of the coil when it is excited by a time varying magnetic field, such as that generated by an RFID tag reader. This voltage could then be used to generate a power supply for the chip. The major unknown with this design was what effect the permalloy shield would have on the incoming magnetic field. There was concern at the outset that the plated permalloy would effectively short the magnetic field away from the coil of wire underneath it. If this were the case, the strength of the field that cut through the plane of the coil would be greatly reduced, and so the voltage at the terminals of the coil would be small.

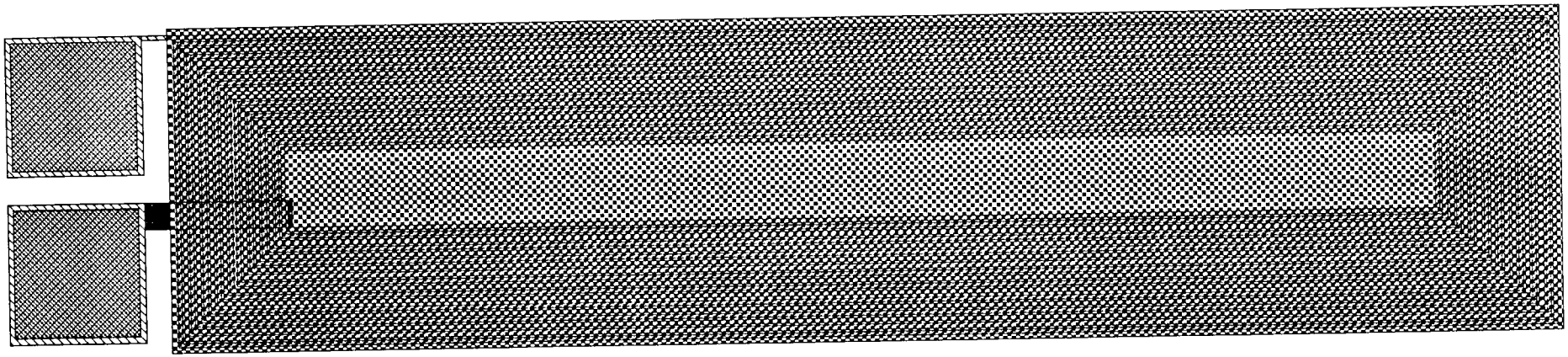
Four different types of LOOPANTs were laid out on NVE's IC layout software for evaluation during this program. They are all essentially the same design, with different shapes and sizes for comparison purposes. Black and white plots of these layouts are shown on the following two pages.


NUEQVIA VIA
NUEQMET2 M2A
NUEQPERM PRA
NUEQWCON WCA
NUEQCORE CRA
NUEQMET3 M3A
LOOPAINT1
LOOPAINT2
LOOPAINT3
LOOPAINT4
M1
VI
PR
WC
CR

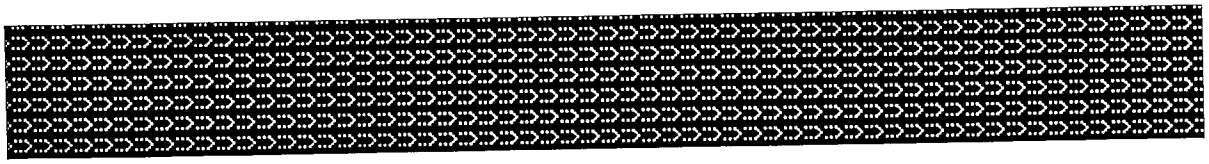


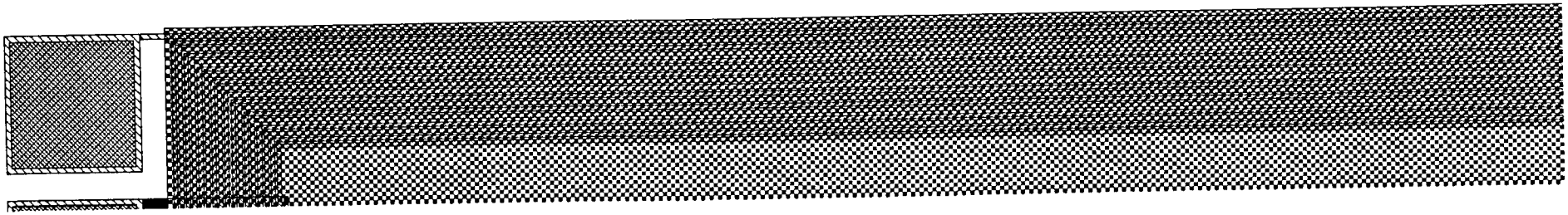
LOOPANT2





LOOPANT3





The area and electrical design characteristics of the LOOPANT devices are summarized in the table below:

Design Name	Silicon Area (Square mils)	Nominal Resistance (Ohms)
LOOPANT1	1275	4753
LOOPANT2	405	1159
LOOPANT3	810	2263
LOOPANT4	1420	4472

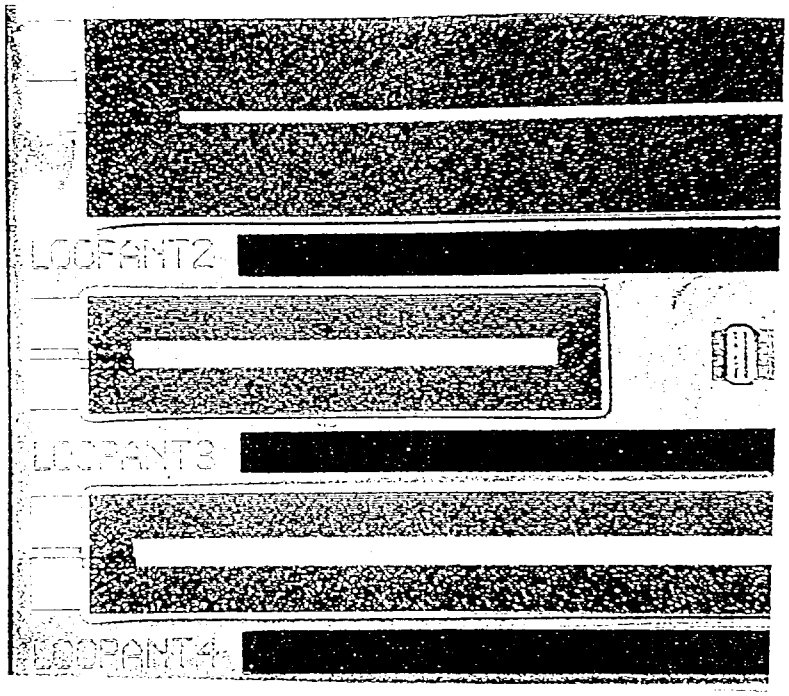
The process used for these devices is the same process that NVE has developed over the last year for plating permalloy shields over the inactive areas of GMR magnetic field sensors. A list of the process steps is given below:

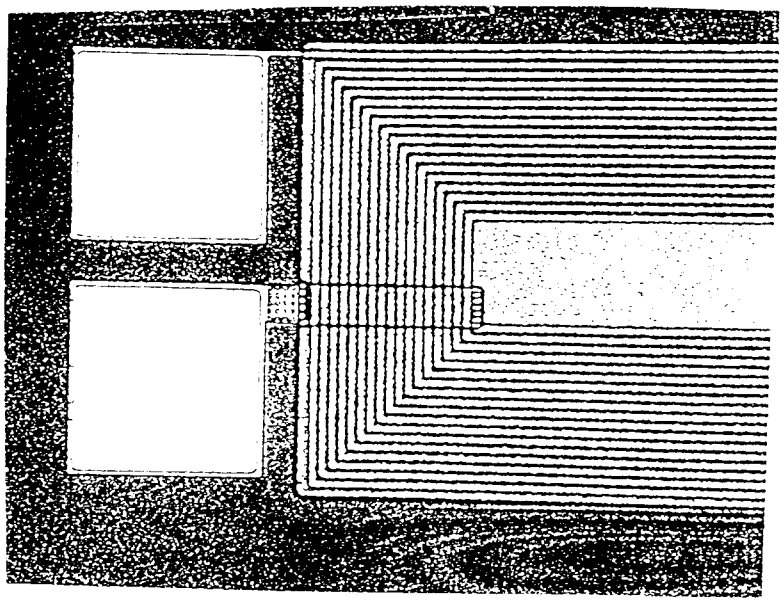
LOOPANT

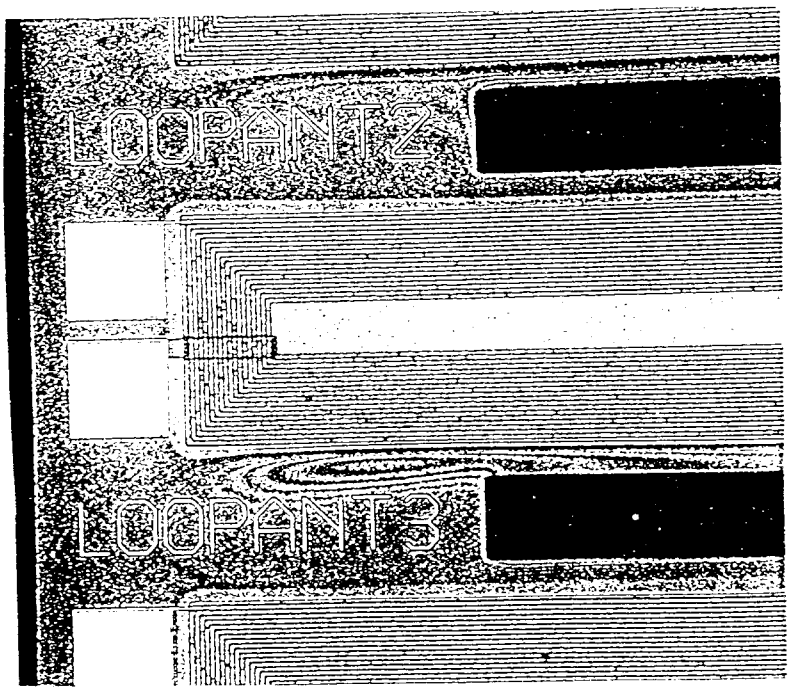
Starting material is 2KÅ LPCVD silicon nitride
M 1 deposition 5KÅ Al/Cu
M 1 photo
M 1 etch wet etch
VIA deposition 7500Å silicon nitride
VIA deposition thickness measurements
VIA photo
VIA etch RIE
VIA etch thickness measurement
M 2 deposition
M 2 photo
M 2 etch wet etch
Dielectric deposition 1 micron silicon nitride
Dielectric deposition thickness measurement
Plating seed deposition 1KÅ permalloy
Core photo 1
Gold plate 1- 2 microns
Gold plate thickness measurement
Core photo 2
Core plate 5 microns permalloy
Core plate thickness measurement
PSV photo

PSV etch RIE
PSV etch thickness measurements
Electrical test

Since no process development was required for this particular device, they came through processing with no problems. The photos below are optical microscope pictures of these devices.



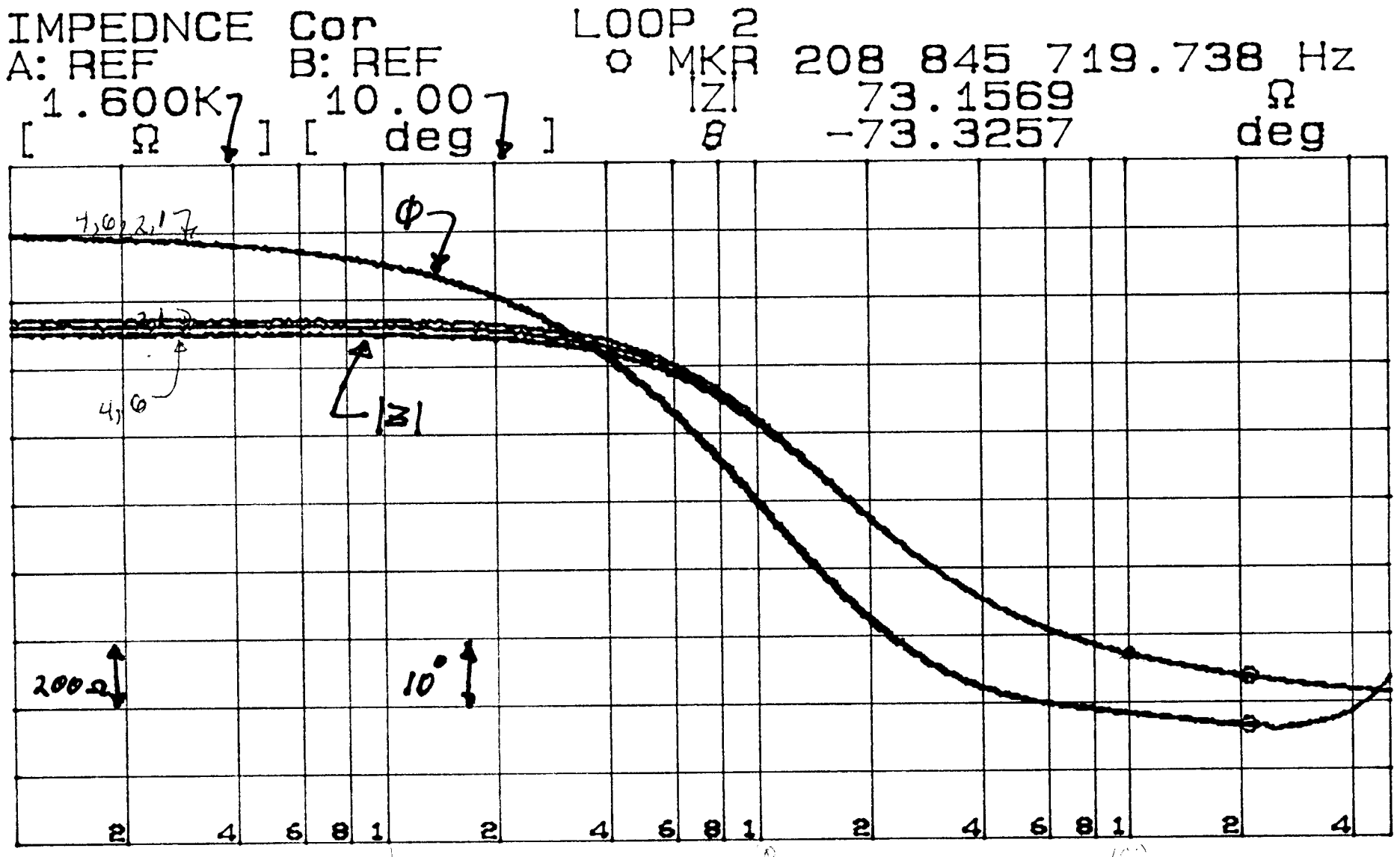




The LOOPANT design was tested initially for design resistance through the coil windings. Actual testing revealed many devices on the wafers that were within +/- 10% of the values shown in the previous table, indicating no shorts between adjacent coil lines, and no breaks in the coil lines. The good devices were then spot checked for inductance values. Typical numbers were on the order of 670 μHenrys for LOOPANT1, 28 μHenrys for LOOPANT2, 84 μHenrys for LOOPANT3, and 620 μHenrys for LOOPANT4. At this point, these devices appeared very promising. When NVE had originally done the electrical calculations for these devices (see Month 3 report), a μ_r of 1 had been assumed as worst case; this led to a calculated inductance value of LOOPANT3 of 2.65 μHenrys. It is clear from the test data that the μ_r is in fact much higher. Actual test data from the four center spots on the wafer are shown on the following page; the voltage across the coil was limited to 0.25V, and the inductance measurements were taken at a test frequency of 1 KHz.

Wafer spot (A,B,C, or D), LOOPANT #	Resistance (Ohms)	Inductance (μHenrys)
A,1	4590	670
A,2	1170	30
A,3	2300	87
A,4	4610	670
B,1	4360	570
B,2	1150	28
B,3	2250	84
B,4	4220	540
C,1	4510	640
C,2	1140	28
C,3	2260	84
C,4	4510	650
D,1	4510	640
D,2	1130	27
D,3	2220	78
D,4	4430	620

Six of these good devices were packaged up and tested for frequency response. The tester essentially applied an RF field of a given frequency and field strength to the packaged devices, while monitoring the terminals for output. The results of the RF test showed no inductive response for the LOOPANT devices. The devices, as seen in the plots labelled LOOP2 and LOOP3 on the following two pages, showed a resistive frequency response characteristic up to a very high frequency (~10 MHz), at which point the impedance dropped due to the capacitance of the package and the die bond wires. NVE had expected to see a peak in the impedance characteristic in the neighborhood of 1-10 MHz as a result of the inductance of the devices, but this did not appear. The first conclusion was that the plated permalloy over the top of the windings was shorting the field in the area and preventing any of the field from going through the middle of the winding loop. The packaged parts were retested with the inductance meter, and surprisingly the results showed no significant inductance. The first guess at the cause of this result, as detailed in the fifth monthly report, was some problem in packaging; however, it was discovered that the test had been conducted without the silicon substrate grounded to one end of the coil. Once this connection was made, the results from the inductance meter returned to their original values.



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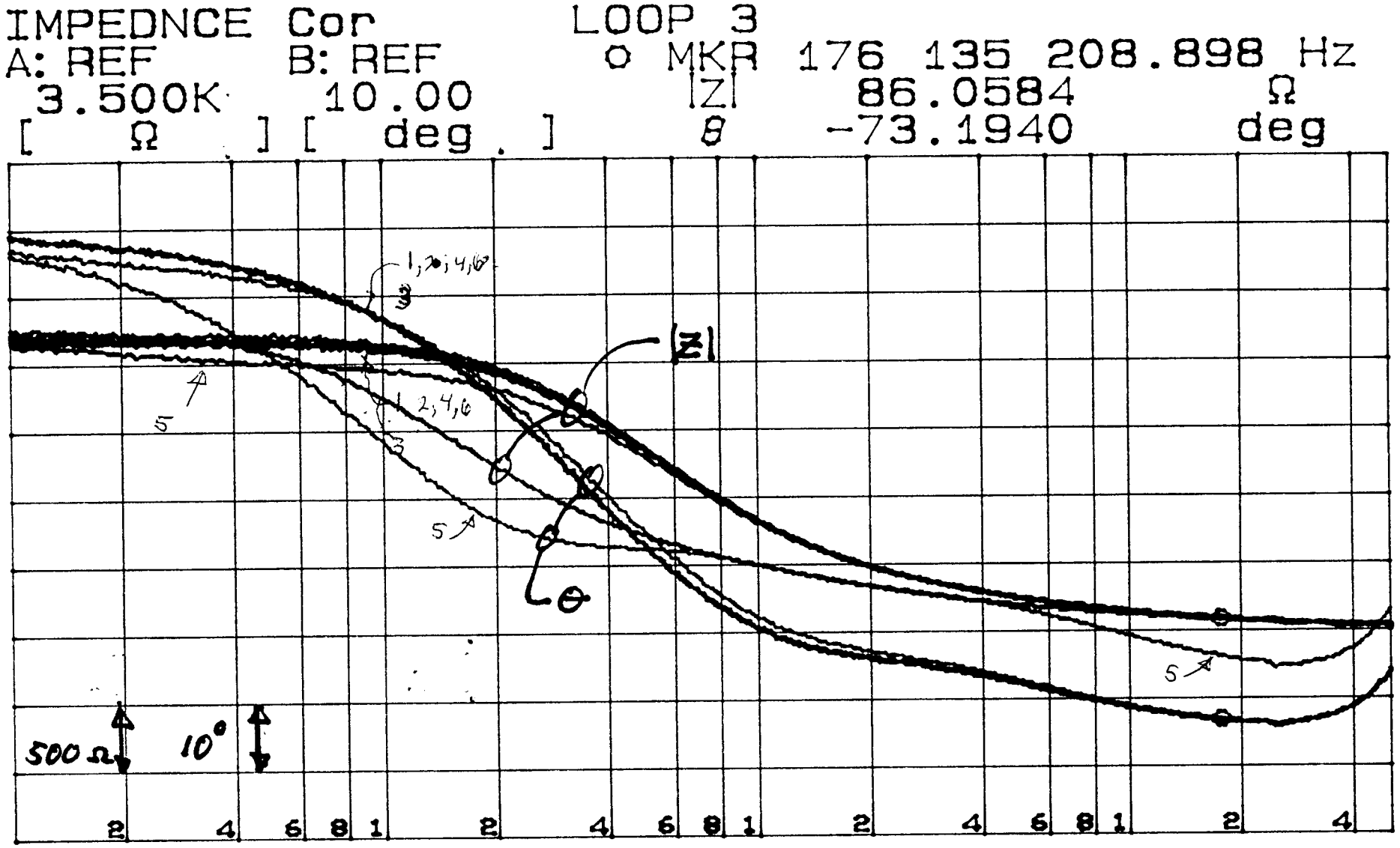

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The conclusions that can be drawn from the experiments with the LOOPANT designs are as follows:

- The process used to make this design is sound
- The devices show a high inductance, but their capture of an externally generated time varying magnetic field is not sufficient for use in an RFID tag application.

2. PLTANT and PLTANTB - The design and mask set for these plated antenna devices is the other design that was described in the original Phase I proposal. These two integrated antennas are identical with the exception of the composition of the Metal-1 layer. PLTANT uses standard semiconductor process metal(98% Al, 2% Cu), while PLTANTB uses copper that is plated, rather than sputter-deposited(both designs use plated copper for the Metal-2 layer). The plated copper layer is about two microns thick, leading to a much lower coil resistance for the PLTANTB devices than the PLTANT devices.

Of all the antenna designs tried during this program, NVE held the highest hopes for this one. It is essentially a duplication of a discrete inductor on a semiconductor substrate, and therein lies the challenge of manufacturing it. The coils of the inductor must loop up and over a thick core of magnetic material. Depositing an insulating layer over the magnetic core, and then depositing the coils so that they climb up the side of the core without breaking through the insulating layer and shorting to the core are extremely difficult challenges for the process engineer.

Because the permalloy core runs through the center of the windings, this design will not suffer from the 'shielding' problem seen in the LOOPANT design. In fact, the function of the core would be to gather a larger amount of flux from the incoming magnetic field. The larger flux density through the coils created by this design would result in a high performance inductor, and make Q multiplication via an RLC resonant circuit possible.

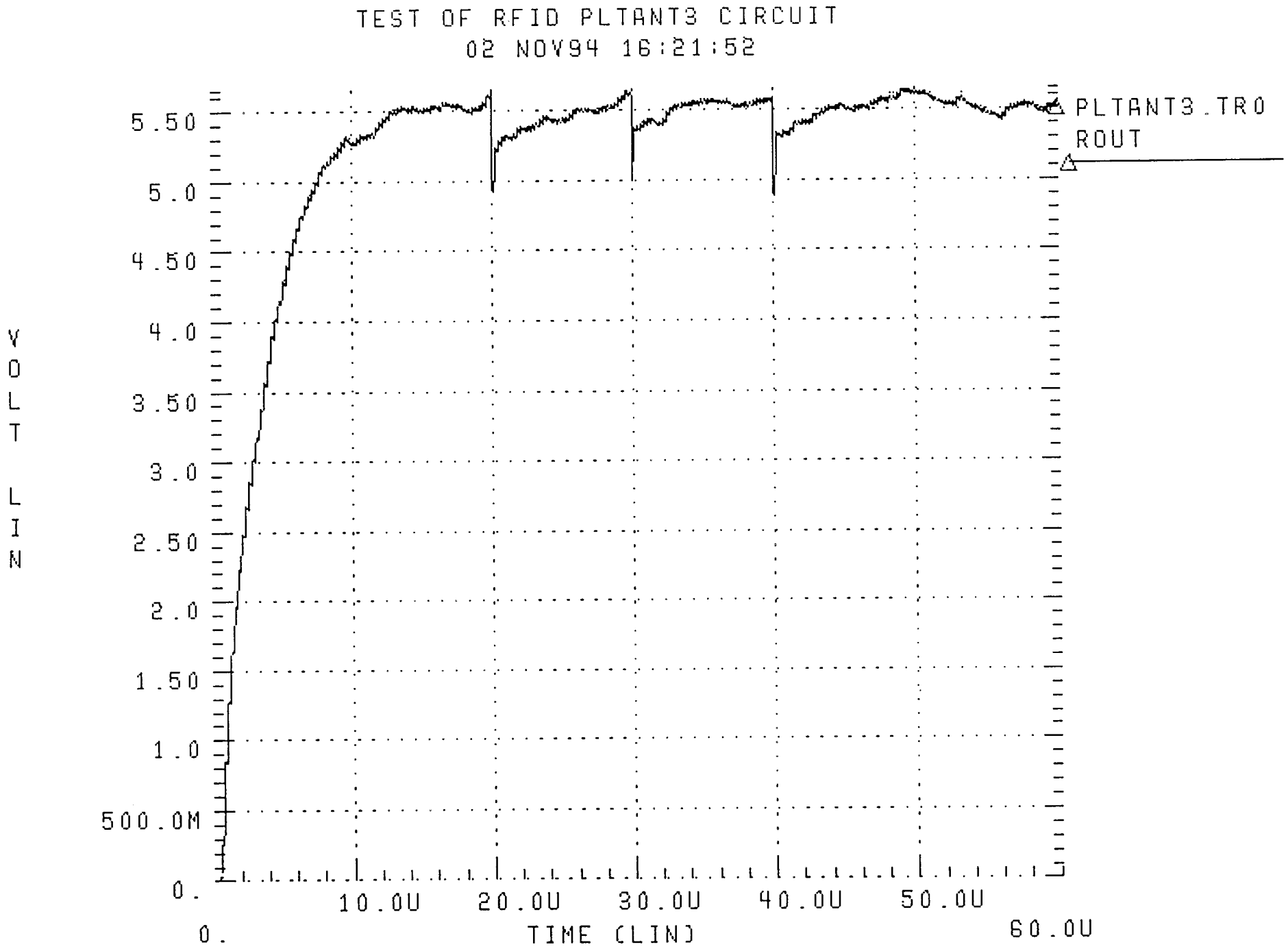
The difference in the PLTANT and PLTANTB devices, as previously stated, is that the PLTANTB devices exhibit a much lower winding resistance than the PLTANT devices; for example, the PLTANT1 antenna has a design resistance of about 159Ω, while the PLTANT1B has a design resistance of

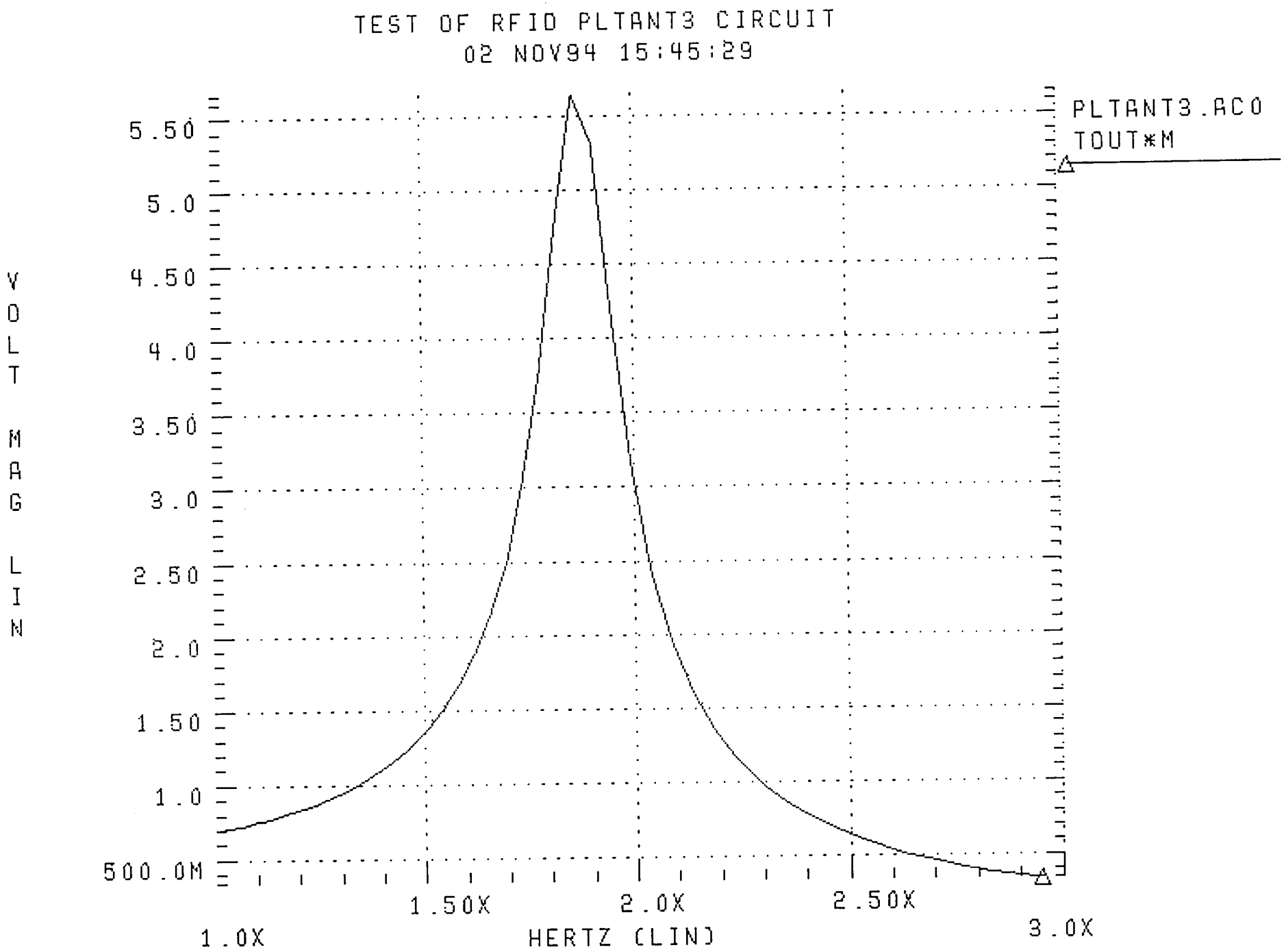
about 19Ω. This allows them to provide a relatively high voltage at the output terminals, at a reasonably low frequency. Typical RFID systems in use today operate at 120 kHz or 400 kHz, with a trend towards moving into the 1.7 Mhz range. NVE did not want to design an antenna that was required to operate at a significantly higher frequency than this. The PLTANT and PLTANTB antenna designs showed peak resonance at anywhere from 800 kHz to 4 Mhz, with voltage outputs in the 5-7 volt range. The results of a typical simulation, showing voltage and frequency response, are provided on the following two pages. The voltage simulation shows a 5 mA current draw, simulating the operation of the chip, occurring every 10 microseconds, for a duration of 50 nanoseconds(read cycle or write cycle operate time). As can be seen from the plot, the voltage on the inductor drops only a half a volt as a result of this load, and the inductor recovers within 10 microseconds, ready for another cycle.

PLTANTs 1 through 4 were laid out on the mask set developed for this program. Like the LOOPANTs, they are essentially the same design, with different external dimensions to provide a variety of inductor sizes. Three black and white plots of these sections of the layout are shown following the simulation plots.

The chip area and design resistance characteristics of the PLTANT and PLTANTB devices are shown in the table below:

Design Name	Silicon Area (Square Mils)	Nominal Resistance (Ohms)
PLTANT1	1440	159
PLTANT2	1925	209
PLTANT3	770	80
PLTANT4	445	40
PLTANT1 (B)	1440	19
PLTANT2 (B)	1925	30
PLTANT3 (B)	770	12
PLTANT4 (B)	445	6


TEST OF RFID PLTANT3 CIRCUIT
02 NOV94 16:21:52
PLTANT3.TR0
ROUT
VOLT LIN
5.50
5.0
4.50
4.0
3.50
3.0
2.50
2.0
1.50
1.0
500.0M
0.
10.0U
20.0U
30.0U
40.0U
50.0U
0.
TIME (LIN)
60.0U


TEST OF RFID PLTANT3 CIRCUIT
02 NOV94 15:45:29
PLTANT3.AC0
TOUT*M
VOLT MAG LIN
5.50
5.0
4.50
4.0
3.50
3.0
2.50
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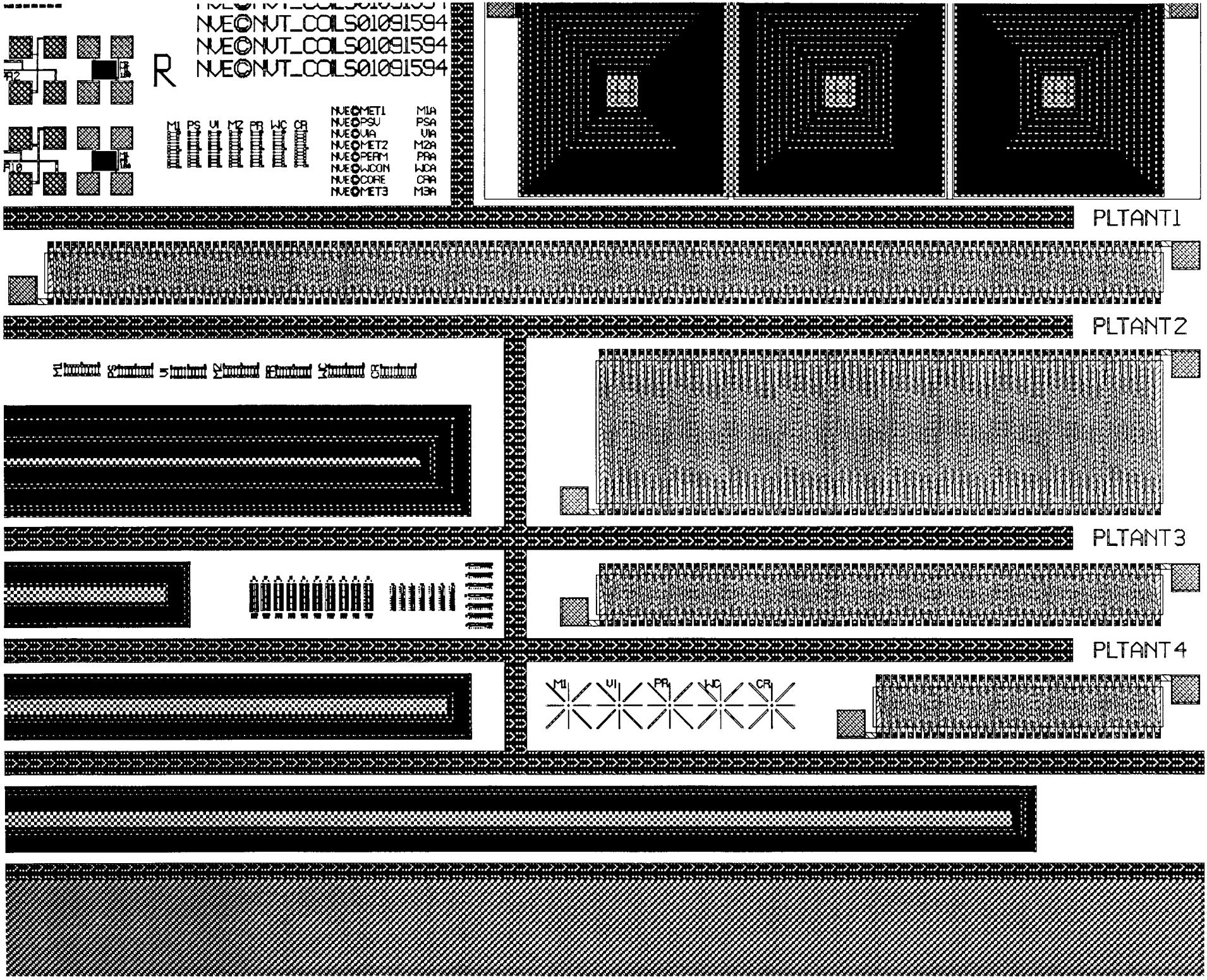
2.50X
3.0X
HERTZ (LIN)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NUE©PSU PSA
NUE©VIA VIA
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NUE©PERM PRA
NUE©WCON WCA
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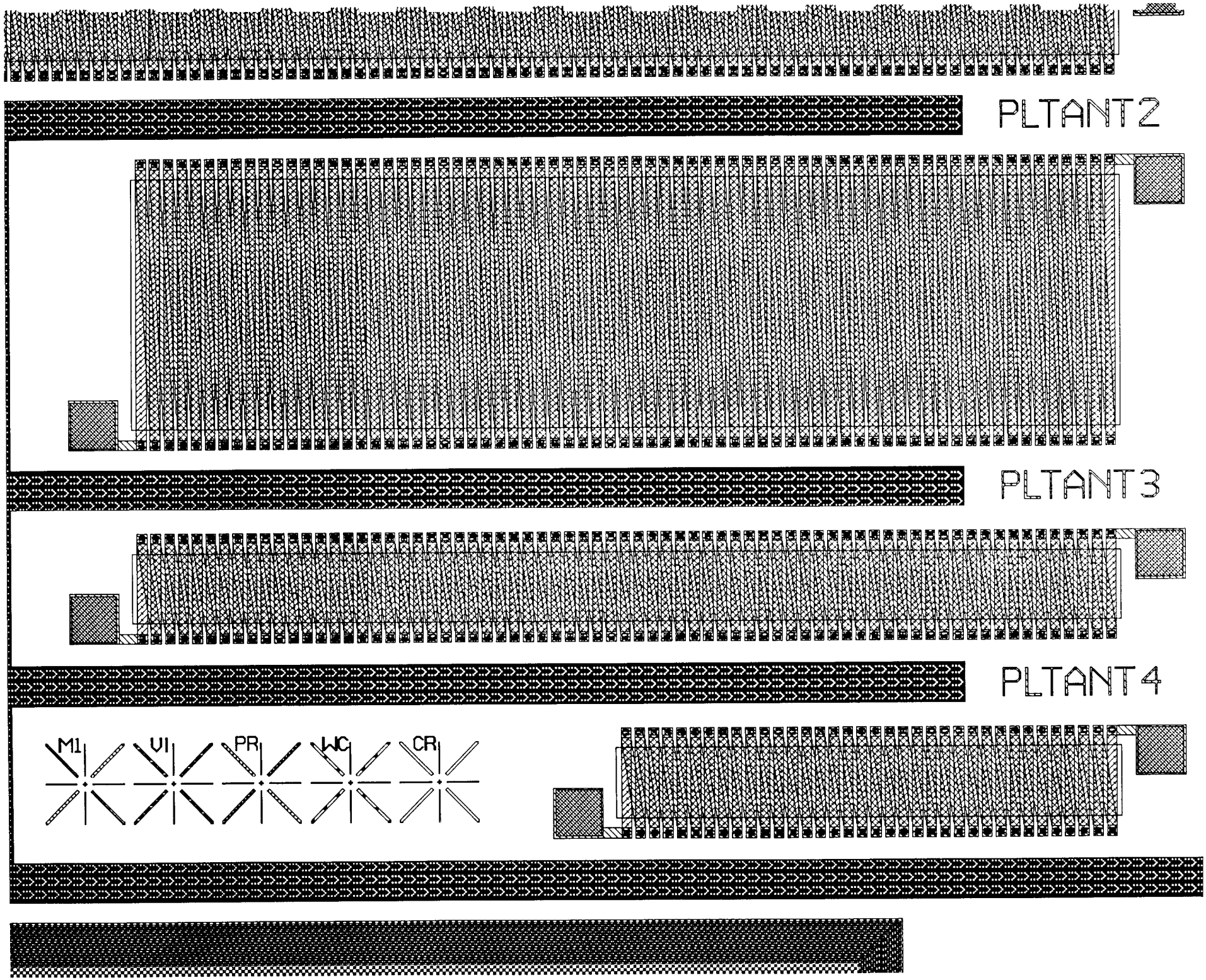
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PLTANT3
PLTANT4
M1
VI
PR
WC
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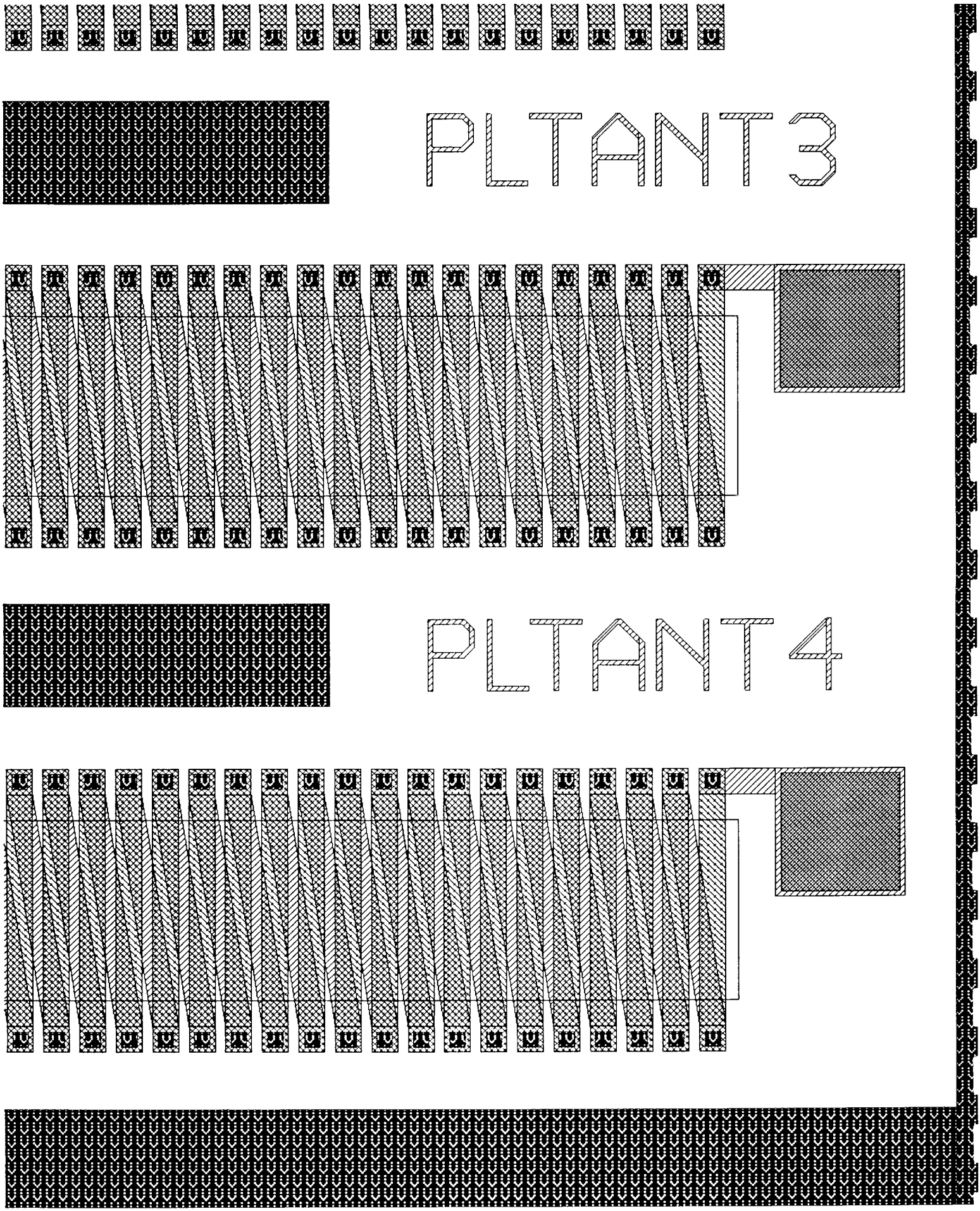

PLTANT3
PLTANT4

The PLTANT and PLTANTB processes used for these devices was developed specifically for this program. A list of the process steps is given below, followed by a brief description of a typical processing run:

PLTANT

Starting material is 2KÅ LPCVD silicon nitride
M 1 deposition 5KÅ Al/Cu
M 1 photo
M 1 etch wet etch
Dielectric deposition 7500Å silicon nitride
Dielectric thickness measurement
Plating seed deposition 1KÅ permalloy
Core photo 1
Gold plate 1 - 2 microns
Gold plate thickness measurement
Core photo 2
Core plate 5 microns permalloy
Core plate thickness measurement
VIA deposition 7500Å SOG/BSQ/silicon nitride
VIA deposition thickness measurement
VIA photo
VIA etch RIE
VIA etch thickness measurement
Plating seed deposition 1KÅ permalloy
M 2 photo 1
Gold plate 1 - 2 microns
Gold plate thickness measurement
M 2 photo 2
M 2 plate 3 - 5 microns copper
M 2 plate thickness measurement
PSV photo
PSV etch RIE
PSV etch thickness measurements
Electrical test

PLTANTB

Starting material is 2KÅ LPCVD silicon nitride
Plating seed deposition 1KÅ permalloy
M 1 photo Mask = NVT_COILS - M4A
Gold plate 1- 2 microns
Gold plate thickness measurement
Dielectric deposition 1 micron BSQ
Dielectric thickness measurement
Plating seed deposition 1KÅ permalloy
Core photo 1
Gold plate 1 - 2 microns
Gold plate thickness measurement
Core photo 2
Core plate 5 microns permalloy
Core plate thickness measurement
VIA photo
VIA etch RIE
VIA deposition 7500Å PECVD SiO2
VIA Deposition thickness measurement
VIA photo
VIA etch RIE
VIA etch thickness measurement
Plating seed deposition 1KÅ permalloy
M 2 photo 1
Gold plate 1 - 2 microns
Gold plate thickness measurement
M 2 photo 2
M 2 plate 3 - 5 microns copper
M 2 plate thickness measurement
PSV photo
PSV etch RIE
PSV etch thickness measurements
Electrical test

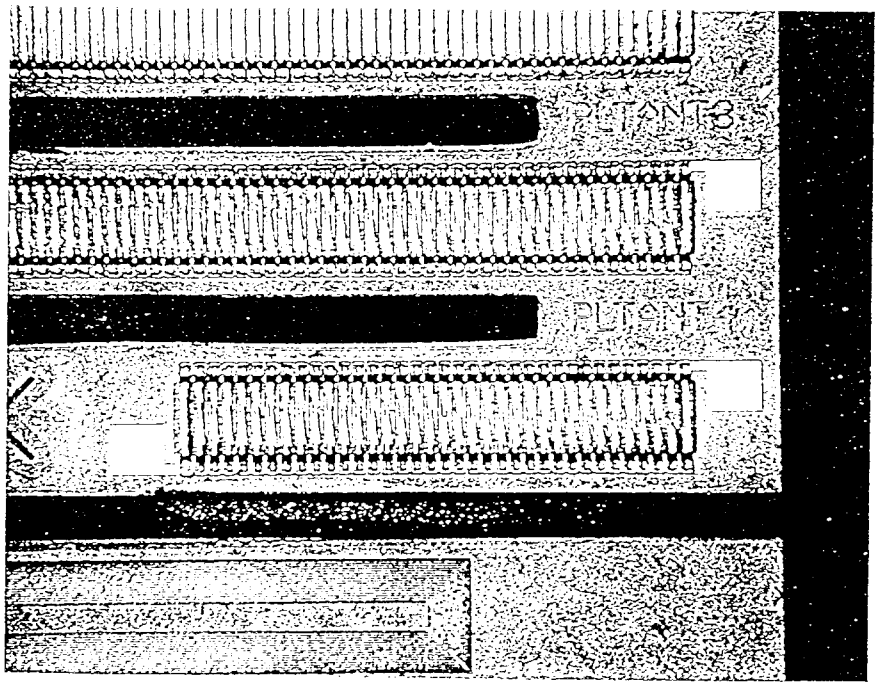
These devices were deposited on 4" silicon wafers, with 2000 Angstroms of silicon nitride insulating material. On the PLTANT wafers, Metal-1(AlCu) is sputter deposited on the entire wafer. Photoresist is then

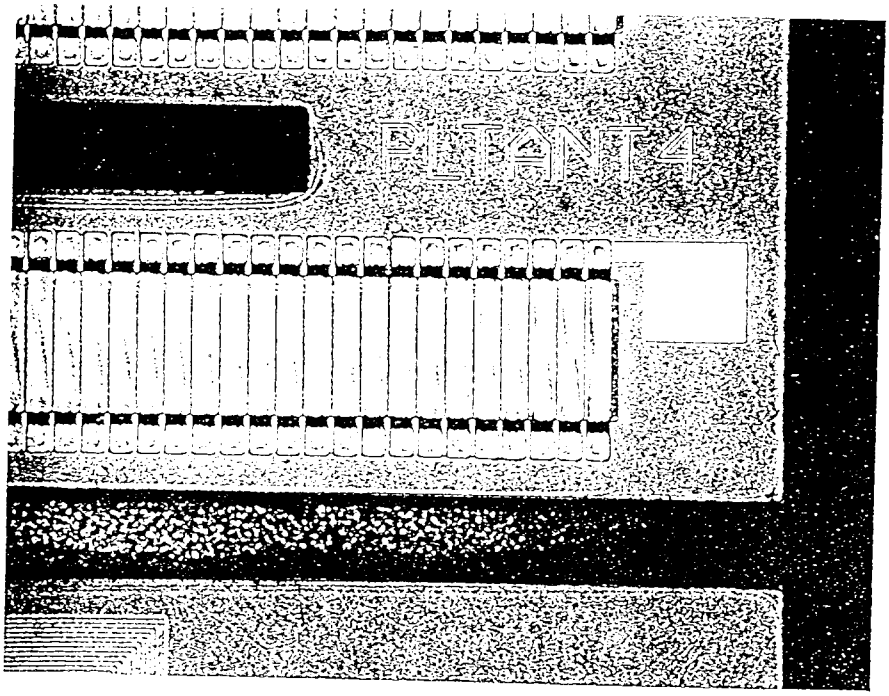
spun on, baked, and exposed with the first mask layer. The Metal-1 is then etched to create the windings under the permalloy core. On the PLTANTB wafers, the photoresist is deposited first, and then gold is plated up through the photoresist to form the bottom windings. From this point forward, the remainder of the process steps for the two types of devices are essentially the same.

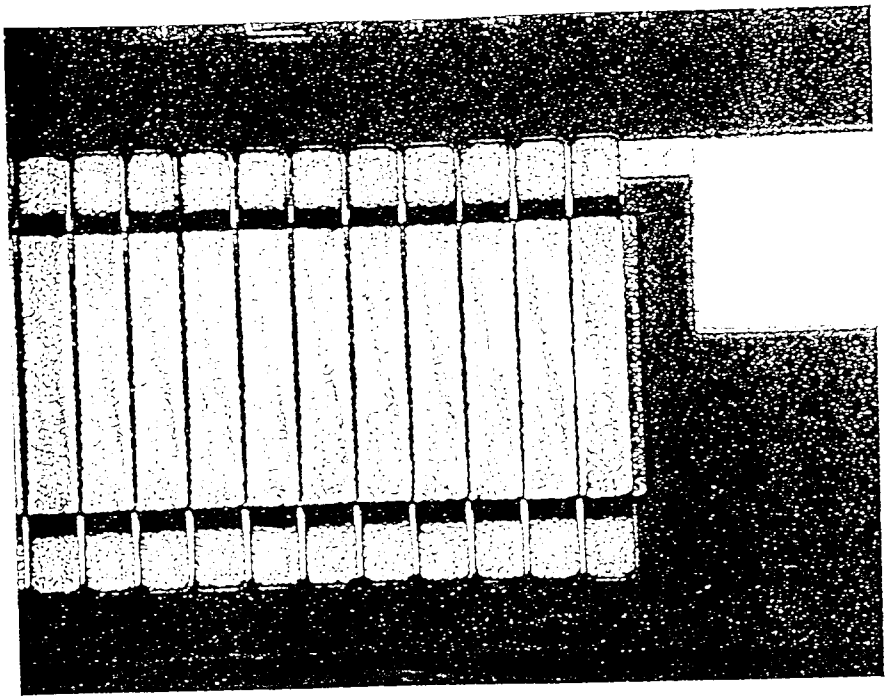
The next step is deposition of an insulating layer of silicon nitride. Then, the next mask layer is used to pattern photoresist for the permalloy core of the inductor. Gold is plated about 1 micron thick up through the hole in the photoresist, for adhesion purposes. The wafer is remasked, this time with a thicker photoresist, and 5 microns of permalloy is plated up through the hole in the resist on top of the gold already plated. The VIA mask layer is then used to pattern photoresist for an etch of the BSQ(Bias Sputtered Quartz) deposited on top of the first windings. This etch essentially cuts holes in the BSQ so that the next metallization layer can make contact to the bottom windings. Next, another insulating layer of silicon dioxide is deposited. This is a critical step, because this layer of SiO2 must cover the top and the sides of the permalloy core, essentially sealing it from electrical contact with the windings. After this SiO2 deposition, the VIA mask is used again to reopen the contacts to the bottom windings(opening these contacts is done in two steps in order to maintain as much silicon dioxide layer thickness as possible).

The photomask for the top windings is used next to define the winding pattern. About 1 micron of gold is plated up through the photoresist. The windings are then remasked, and 3 to 5 microns of copper is plated on top of the gold. This thickness is determined by the height of the core; if the permalloy core were 10 microns thick, 10 microns of copper would be required for the windings. The most critical area of this deposition is the step where the top windings passes over the step created by the permalloy core. Some thinning of the nitride layer and the top winding can be expected, and too much of it may result in either shorts to the permalloy core, or open windings. The last step in the process is a mask step and etch of the nitride layer over the bonding pads, so the device can be probed or bonded out in a package.

The photos on the next two pages were taken with NVE's optical microscope, and show various views of the completed PLTANT and PLTANTB devices.


PLANTS
PLANT


PLANT

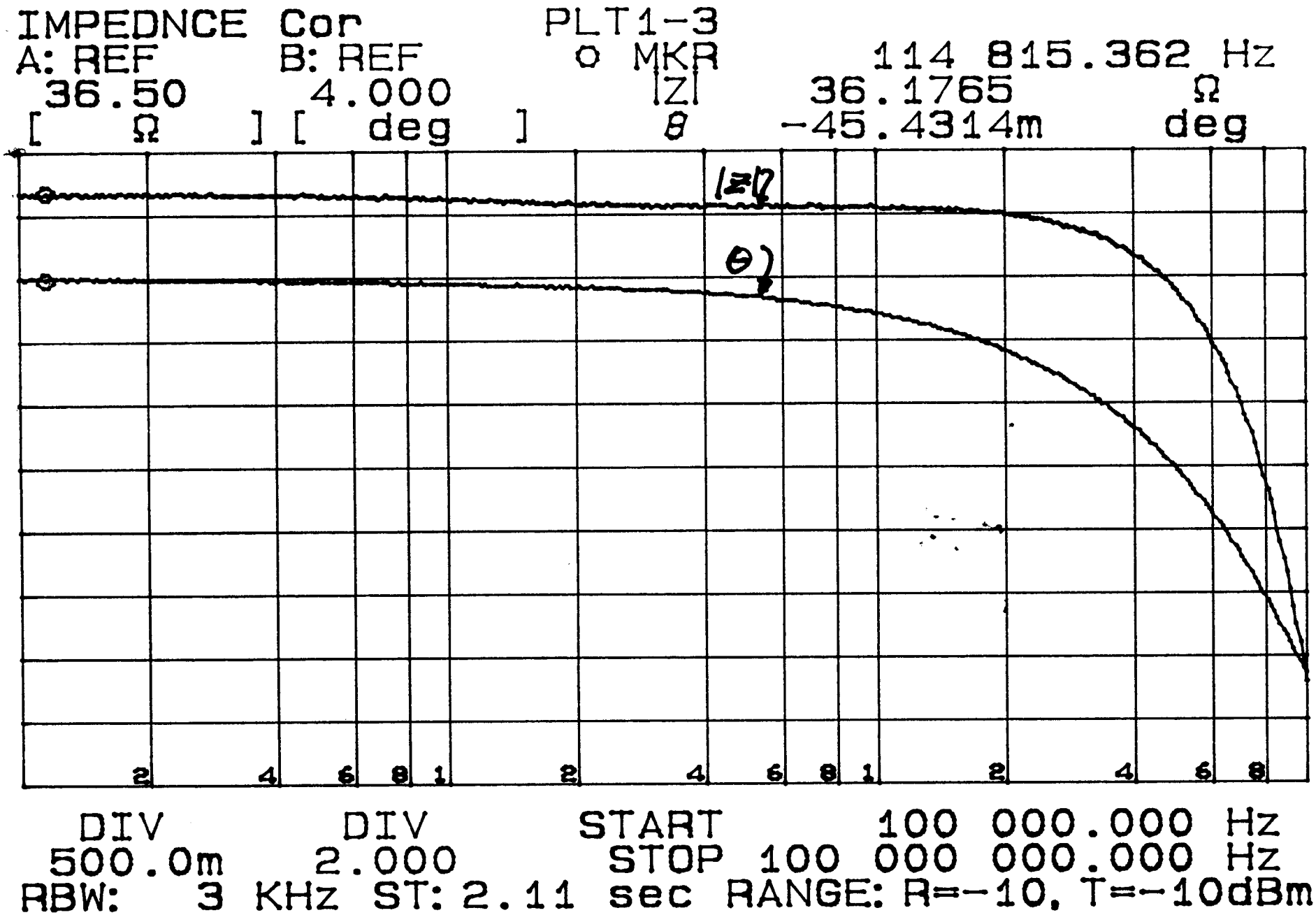


The PLTANT and PLTANTB devices showed a much lower yield than the LOOPANT devices, which is consistent with the difficulty of the processing steps associated with these devices. The wafer containing the PLTANT devices contained virtually no devices which would pass the resistance measurement test. Almost all devices tested as dead shorts. NVE process personnel were not surprised, because this wafer was the first one through the process line, and certain process parameters such as etch rates were tested on this wafer, and then adjusted for subsequent wafers. The PLANT devices seemed to show missing dielectric between the core and the windings of the device, which would allow the current to short to the core; this leads to no current going through the windings around the core, and therefore no inductive effect. Visually, the PLANTB devices looked much better with no evidence of this shorting; however, most of the devices on this wafer also appeared as dead shorts. There was an area in the top center of the wafer where the devices looked like they had the proper resistance, so these devices were tested for inductance values. The tests showed almost no self inductance, which indicates that there was still shorting either between the coil windings or from the coil windings to the core. The resistance of these devices turned out to be simply a more resistive short than seen on the other areas of the wafer.

Six of each type of these devices were packaged up and tested with a variable frequency RF generator like the one used to test the LOOPANTs. This was done essentially as a check against the static measurements made in the test lab. The results are shown on the following three pages; the plots of the output are labelled PLT 2-4, PLT 1-3, and PLT 3-6. These results showed a purely resistive response until very high frequencies, where the capacitance and inductance of the die bond wires came into play. Again, NVE expected to see a peak in the 1-10 Megahertz range as a result of increasing impedance due to the inductor, but no peak was observed.

Since these parts were the ones expected to perform best in the actual application, NVE undertook a detailed failure analysis effort to determine why these parts did not work properly. One problem became clear when the parts were probed at wafer test. As NVE had suspected, shorts were apparent between the windings of the coil and the permalloy core. The test that conclusively proved this to be the case involved taking one wafer probe and contacting a winding, while another one was used to make contact to the end of the permalloy core. Contacting the core required scraping away the layer of silicon dioxide that had been deposited on top of it; this was done using a very strong probe tip. Electrical resistance of less than 10 Ohms was observed on all the devices that were tested in this fashion, leading to the irrefutable conclusion that the windings were shorted to the core. Visual evidence of this problem was also found on close inspection with an optical microscope. The edges of the permalloy bar that forms the core appeared shinier than the middle sections, and adjacent to the shiny edge was a boundary that looked rough and bubbly(these contrasting features do not reproduce well in photographs, so none have been included in this report). NVE believes these visual features correspond to where the silicon dioxide was completely stripped away during processing(shiny area), and the edge of the remaining silicon dioxide on the permalloy core(rough, bubbly area).

After looking at the photoresist profile on top of the permalloy core, NVE believes it has identified the cause of this problem. When photoresist is spun on the wafer during the second VIA mask step, it does not form a layer of uniform thickness on top of the core. The photoresist is designed to provide uniform thickness over a relatively planar surface, but the 5 or 6 micron high permalloy core protrudes through the photoresist like a tall building constructed on a very flat plain. There is photoresist present on the top of the core, but it is not uniform in thickness; it tends to become much thinner at the edges.



Duggan 1-10-95

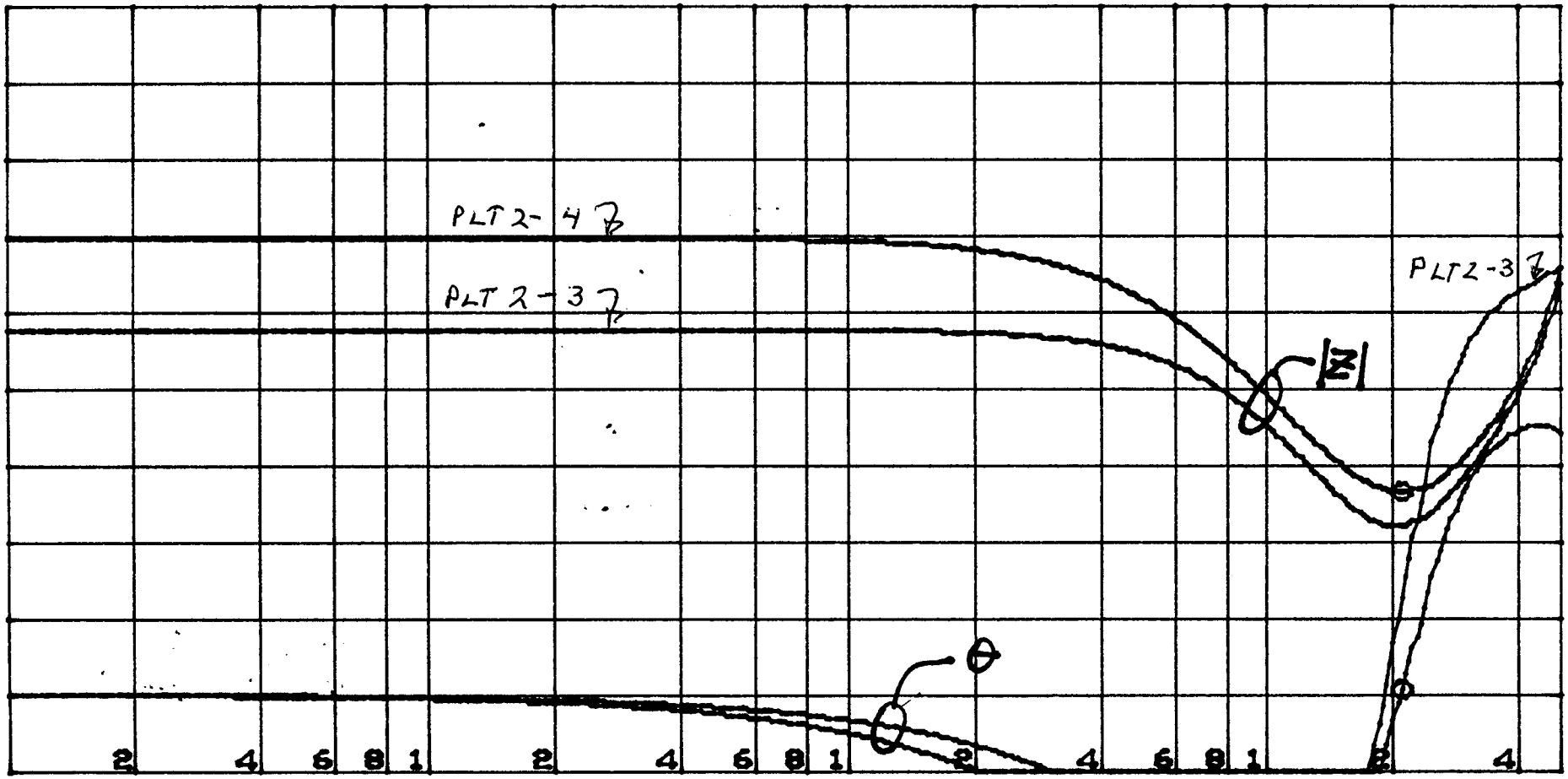
2-4

IMPEDNCE Cor PLT 2-4

A: REF B: REF ○ MKR 208 845 719.738 Hz

80.00 90.00 |Z| 16.5329 Ω

[Ω] [deg] θ 826.541m deg



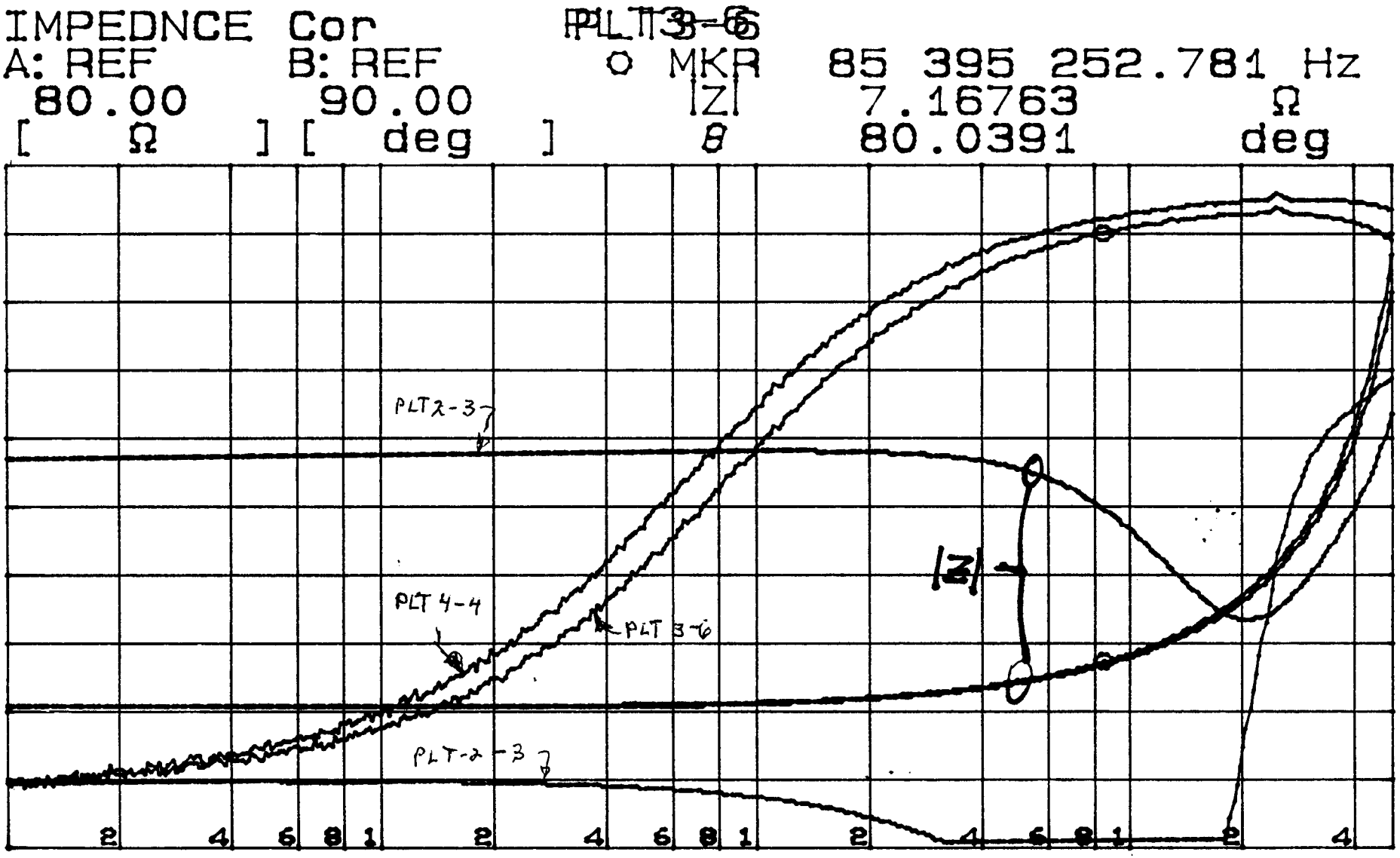
DIV DIV START 100 000.000 Hz

10.00 10.00 STOP 500 000 000.000 Hz

RBW: 3 KHz ST: 2.11 sec RANGE: R=-10, T=-10dBm

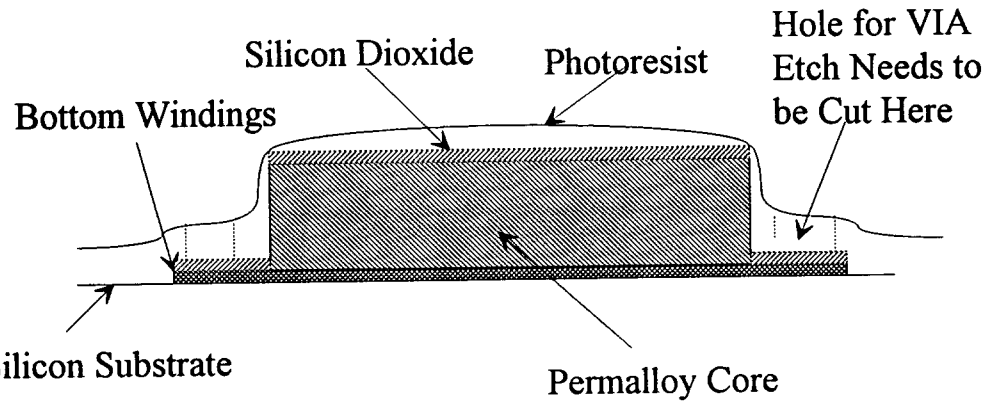
RBW: 3 KHz ST: 2.11 sec RANGE: R=-10, T=-10dBm

Duggan 1-10-95



Duggan 1-10-95

The drawing below shows the relative thickness of the photoresist layer at various points on the wafer; notice the thinning of the photoresist near the edges of the permalloy core:

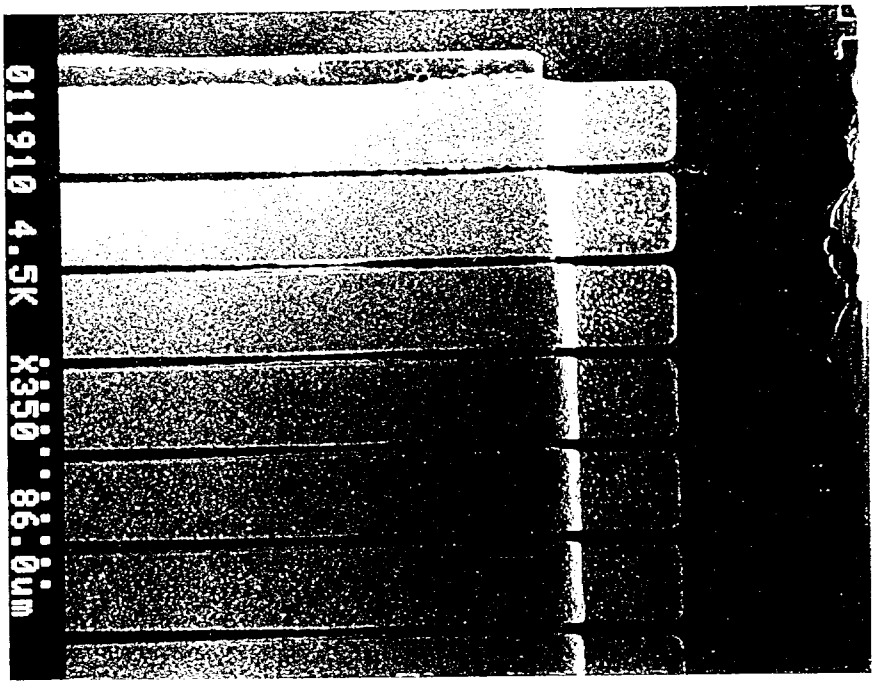


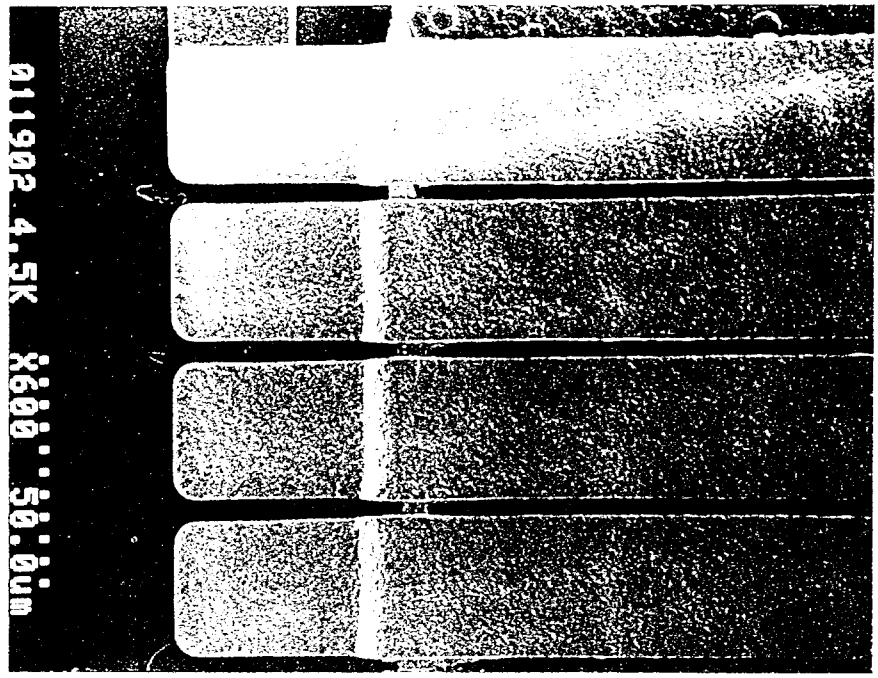
After the photoresist is patterned and developed, NVE uses a reactive ion etch process (RIE) to cut the holes in the silicon dioxide layer. The RIE process is very accurate for small contacts, but does not provide a preferential etch rate for the photoresist versus the SiO2. Therefore, when the etching took place on these devices, the thin layer of photoresist over the edges of the permalloy core was etched away almost immediately, and the silicon dioxide on these edges began to be etched as well. By the time the contact hole was completely cut, the entire layer of SiO2 had been removed at the edges of the permalloy core.

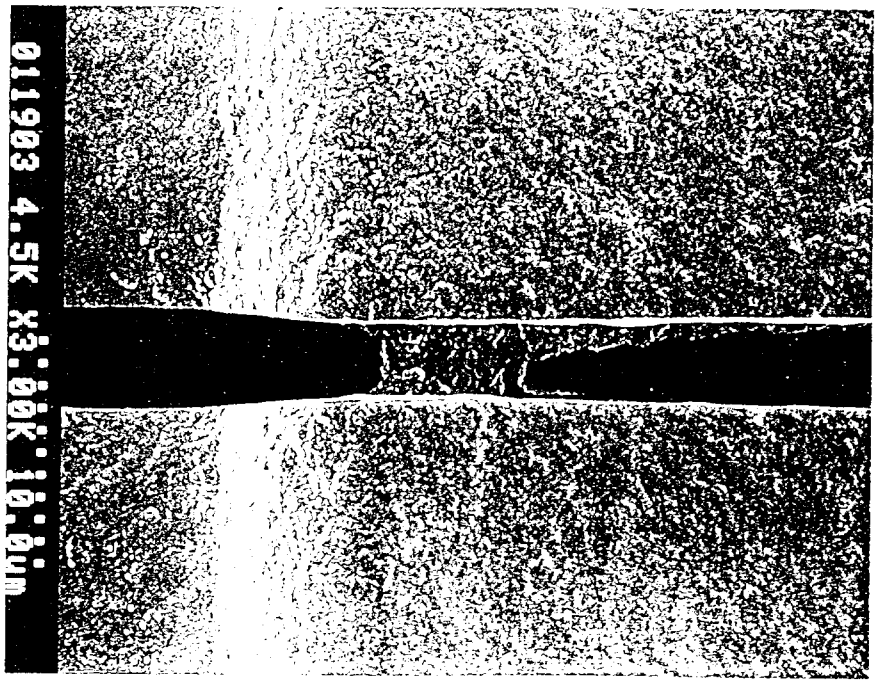
The fix for this problem is a process change to a wet etch, rather than an RIE. Wet etches are not able to open very small contacts, but the contacts required by this device are so large (>10 microns square) that a wet etch will work fine. The advantage offered by a wet etch is a 5:1 or 10:1 preferential etch rate. In other words, the etch will work on silicon dioxide five to ten times faster than it will work on photoresist. Using this process, the thin areas of photoresist near the edges of the permalloy core should survive long enough to protect the layer of SiO2 there.

As part of the failure analysis process, NVE had scanning electron microscope(SEM) photos taken of the devices produced during this work. An unexpected problem became apparent from these photographs. In addition to shorts between the windings and the core, shorts also appeared from winding to winding. The following photos show winding to winding shorts and near shorts.


011909 4.5K X250 120um


011910 4.5K X350 86.0um


011902 4.5K X600 50.0um


011903 4.5K X3,000K 10.0um

The shorts essentially fall into two different categories. The first two photos show variations in the winding line width in the center area of the core. The second two photos show shorts at the edge of the core, adjacent to the vertical wall. There are two different mechanisms at work here. The shorts in the center of the core area contrast markedly with the separation distance shown by the windings on the surface of the silicon wafer. This indicates a photolithography problem. This is easy to understand considering the difference in heights on the wafer surface; the top of the permalloy core is 5 or 6 microns above the wafer surface. The GCA 10X stepper that NVE uses for photolithography operations has a depth of field of about 2 microns. This means that when the surface of the wafer is in focus, the area on top of the core is slightly out of focus. NVE believes that the out of focus condition led to line width variation on top of the core, which resulted in the shorting in the center area. The shorts near the edges of the core are most likely the result of the etchant liquid not staying in the proximity of the gold and copper long enough to etch completely through the metal.

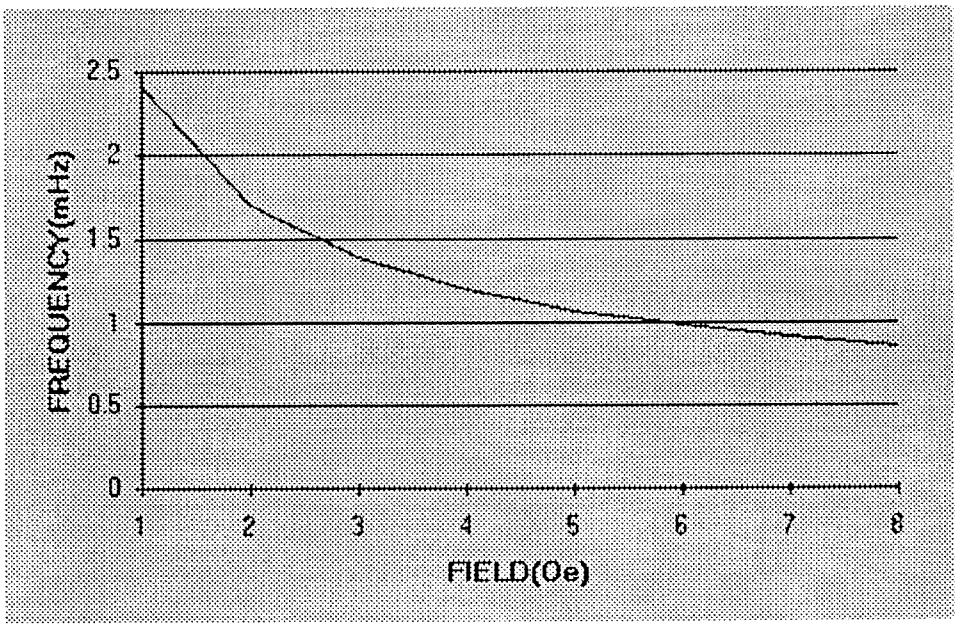
These two problems can both be addressed in a straightforward way. In order to compensate for the out of focus condition on top of the core, the mask design should be changed to allow a greater distance between the windings. Five microns was used with the mask set developed for this program, so 10-15 microns should provide the safety margin required. The other problem can easily be fixed by increasing the etch time by 5% or 10%.

As a result of this Phase I program, NVE has drawn the following conclusions about the plated antenna design:

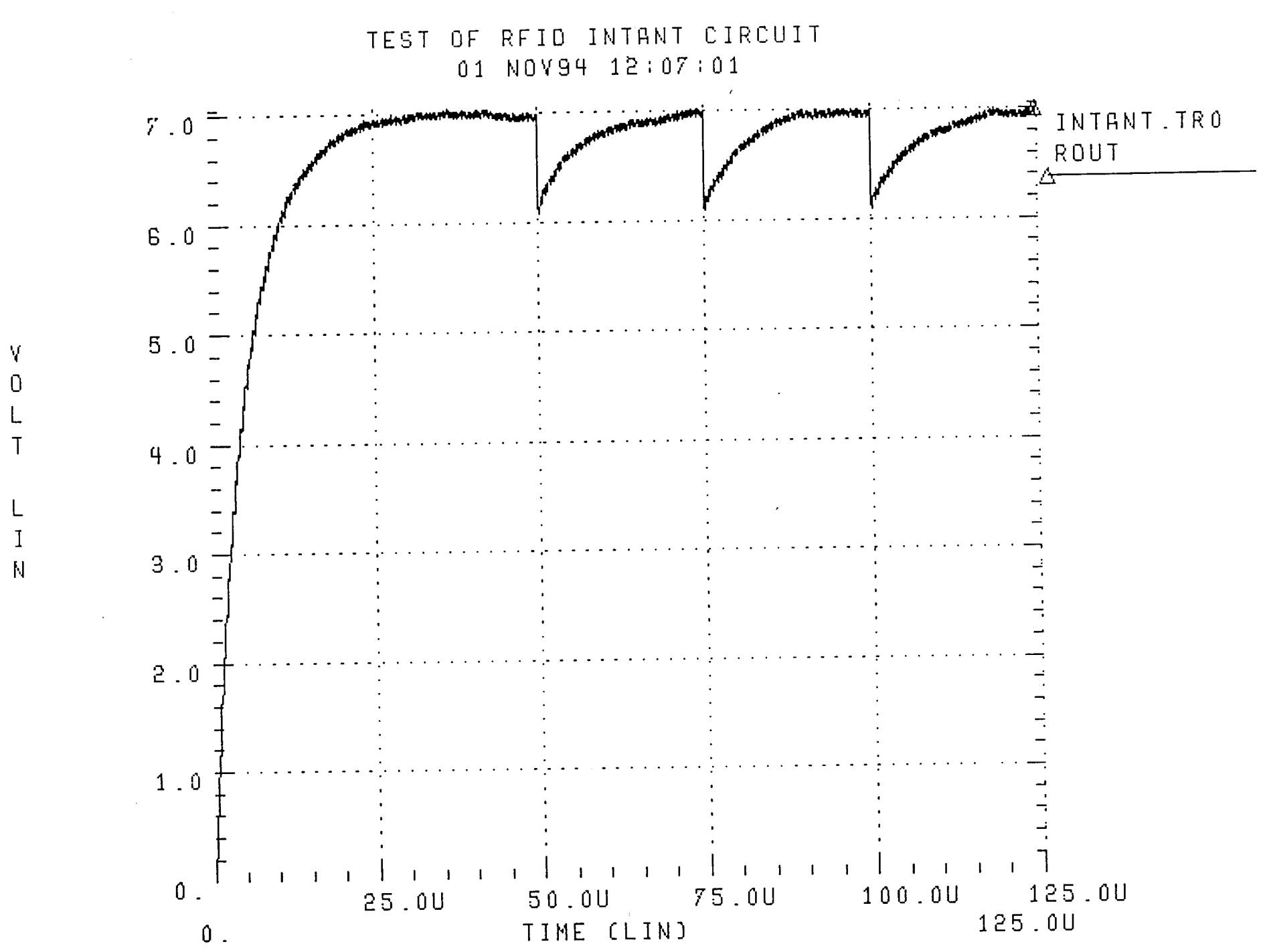
1. Electrical simulations conclusively show this design to be most desirable in terms of providing power to an RFID chip.
2. Processing problems prevented successful manufacture of this design.
3. The processing problems have been conclusively identified, and alteration of the process steps previously described, along with a mask redesign, is likely to result in functional parts.

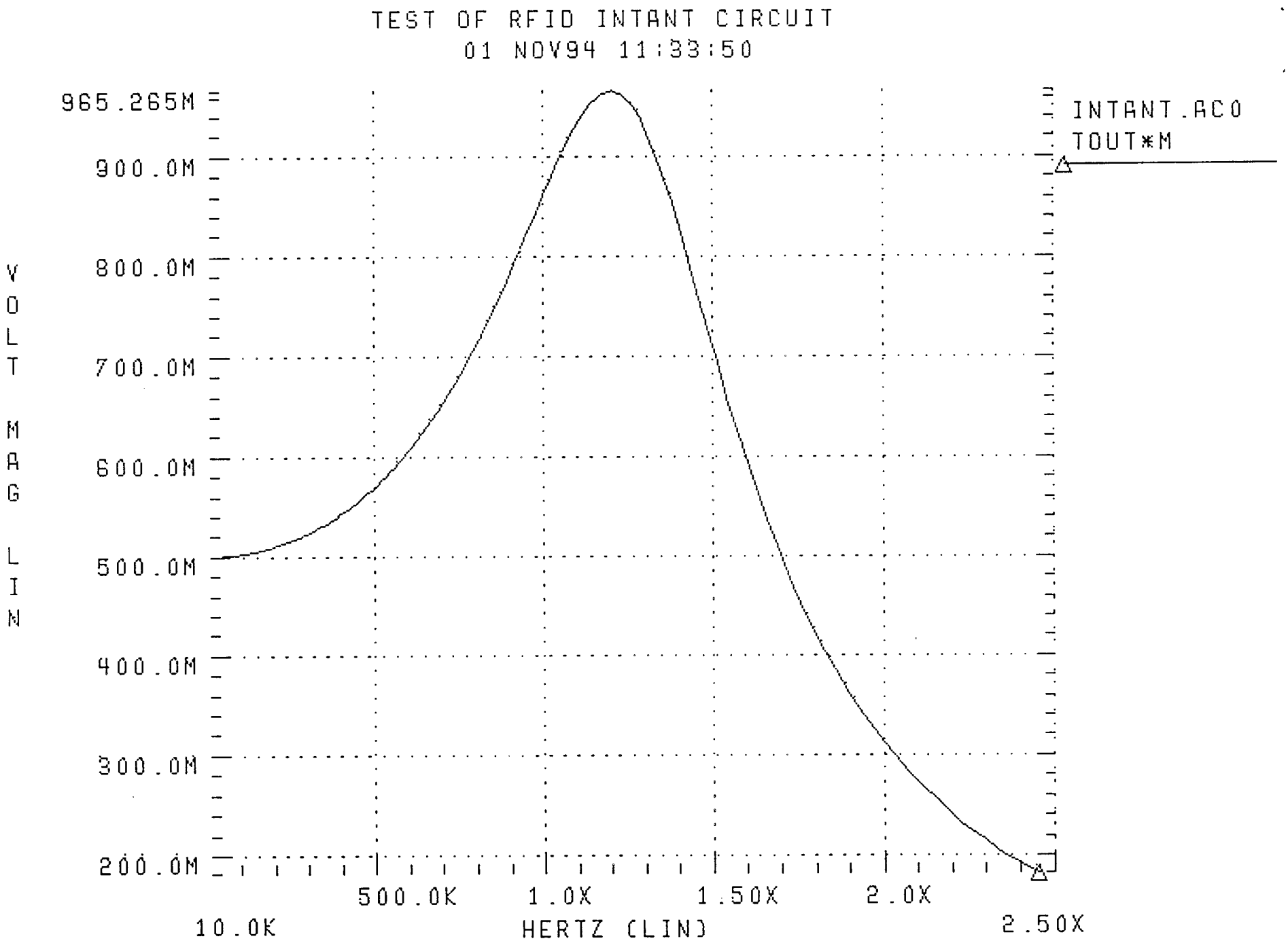
3. INTANT - This device is one that NVE invented after the Phase I proposal was already submitted. It involves a two level plated permalloy core, and a large number of windings deposited on top of the first level. The large resistance of these windings limits the Q multiplication of the voltage output from this inductor; however, the magnetic field cutting through this large number of windings should provide a high voltage level at a reasonably low frequency; in effect, no significant amount of Q multiplication would be required. NVE also felt that this design may be easier to process than the PLTANT design, because no windings were required to cross over the large step at the edge of the permalloy core.

Using the geometrical parameters designed into these devices, NVE calculated the inductance of this device to be 434 μHenrys. Using this number, and the calculated resistance value of about 1900 Ohms, HSPICE simulations were run to determine if this device could be made to operate given the magnetic field available at the chip. The results of the simulations are shown on the following two pages, and clearly indicate that this is a promising design. These simulations were the result of an input frequency of 1.2 Mhz, and a field strength of 4 Oersteds; however, this device should be functional over a relatively broad range of frequencies, as indicated in the graph below:



This graph indicates that the range of this design would be less than the PLTANT1 and PLTANT3 designs, which require only 1 and 2 Oersteds at lower frequencies. However, the field strength available at the


TEST OF RFID INTANT CIRCUIT
01 NOV94 12:07:01
INTANT.TRO
ROUT
7.0
6.0
5.0
4.0
3.0
2.0
1.0
0.
VOLT
LIN
0.
25.0U
50.0U
75.0U
100.0U
125.0U
TIME (LIN)
125.0U

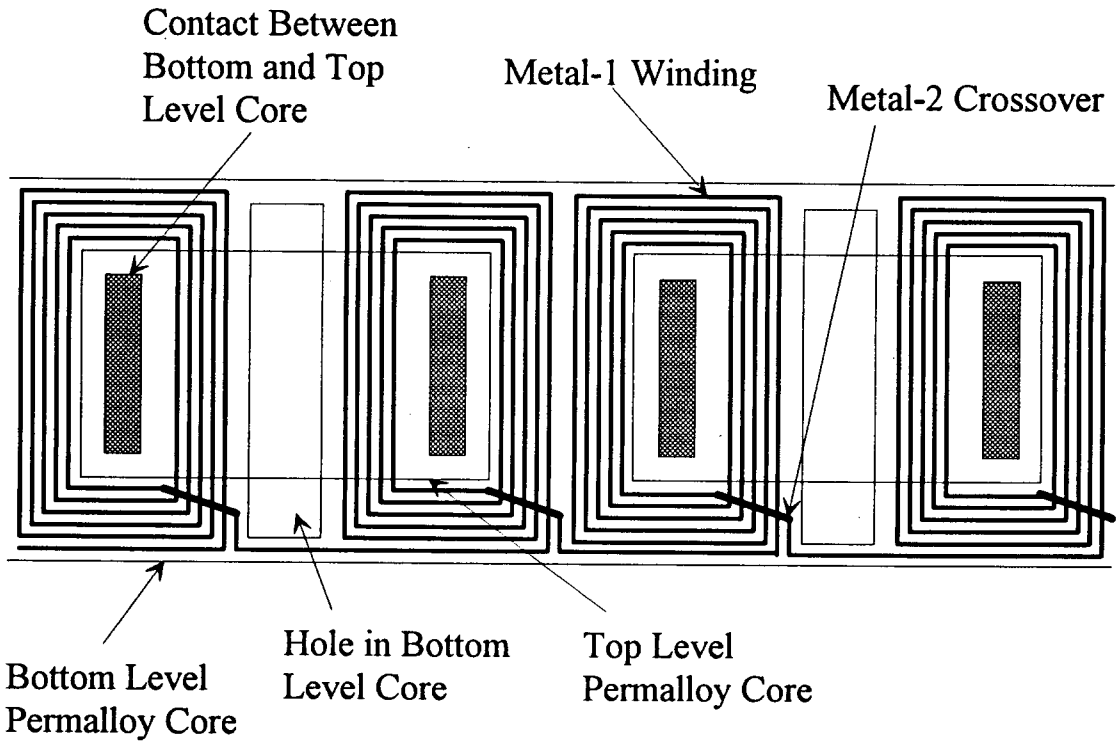

TEST OF RFID INTANT CIRCUIT
01 NOV94 11:33:50
965.265M
900.0M
800.0M
700.0M
600.0M
500.0M
400.0M
300.0M
200.0M
VOLT MAG LIN
INTANT.AC0
TOUT*M
10.0K
500.0K
1.0X
1.50X
2.0X
2.50X
HERTZ (LIN)

face of a typical hand-held RFID reader is about 10 Oersteds, so this design is definitely workable.

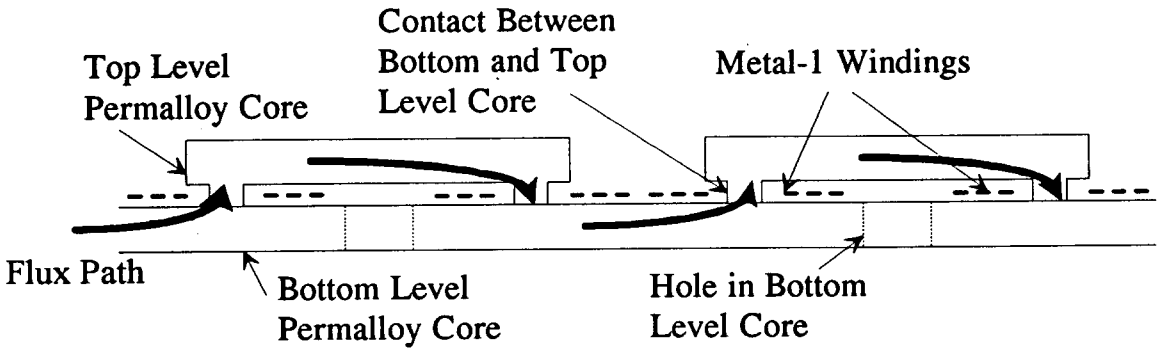
One improvement for this design was proposed during the Phase I work. This would involve adding more coils by using more Metal-2 on top of Metal-1. As the design is laid out, Metal-2 is only used for a crossover; its use could be expanded so that it essentially duplicated the Metal-1 structure. By adding to the number of coils, the frequency of operation could be reduced for the same tank circuit output voltage. The only drawback is an increase in the size of the tank circuit capacitor required, but this capacitor is so small that it could be easily implemented on the chip itself.

Top and side view drawings that show the basic construction of this design are provided below:

Top View



Side View

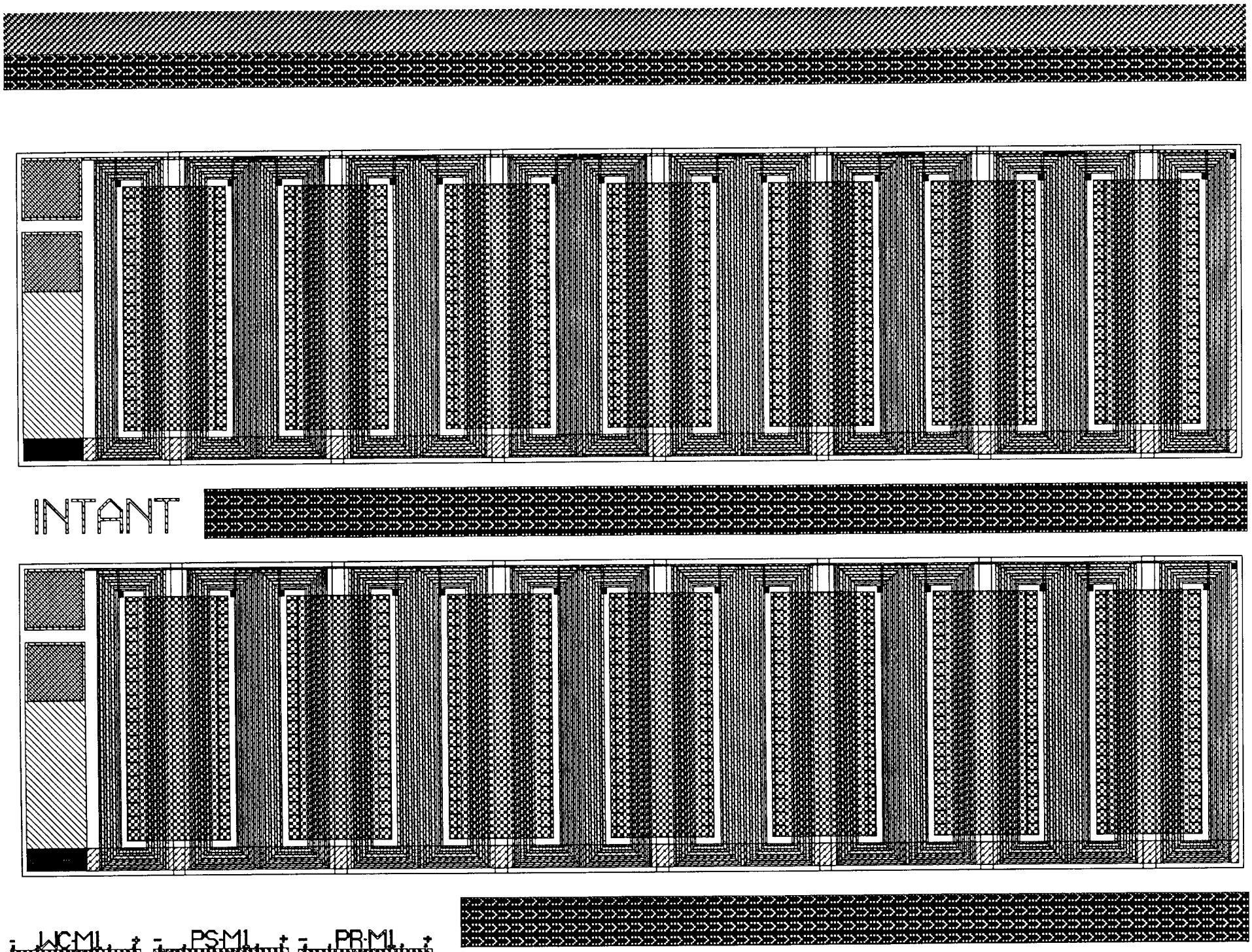


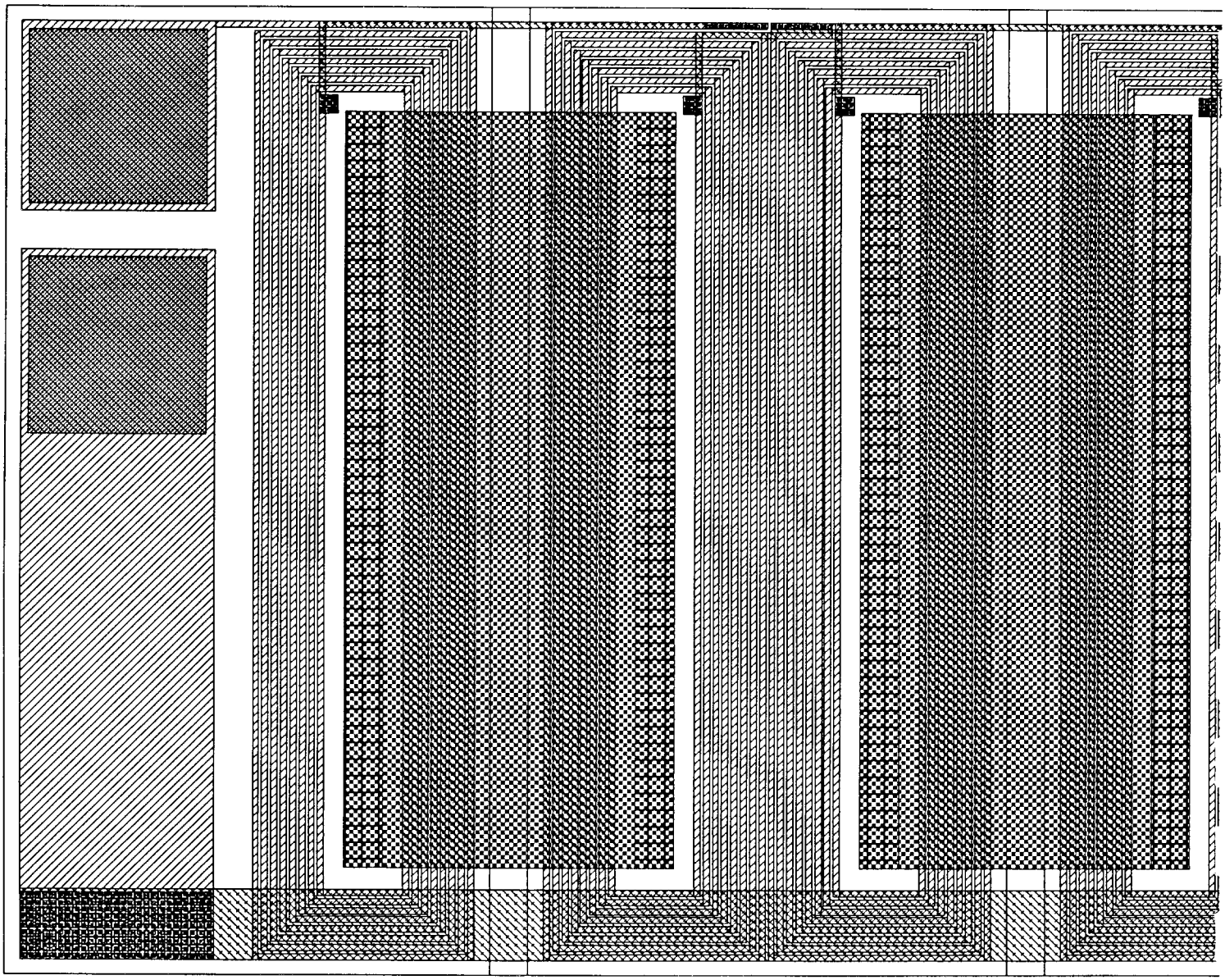
The flux path shown in the side view drawing cuts through each coil of windings on top of the bottom core. The hole in the bottom core makes the lowest reluctance path as shown; if the hole were not there, a good percentage of the flux would travel only through the bottom core, bypassing the windings.

Two identical devices were laid out on the mask set. Plots of the design are shown on the following three pages. The bond pads for these devices are positioned on top of the bottom core. When integrating a device such as the INTANT onto a semiconductor substrate, bonding wires would be required to connect the power pads on the substrate to the bond pads on the bottom core.

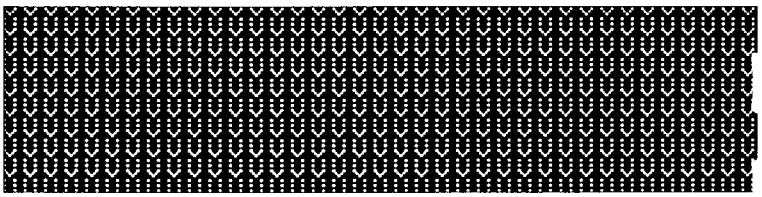
The area and electrical design characteristics of the INTANT devices are summarized in the table below:

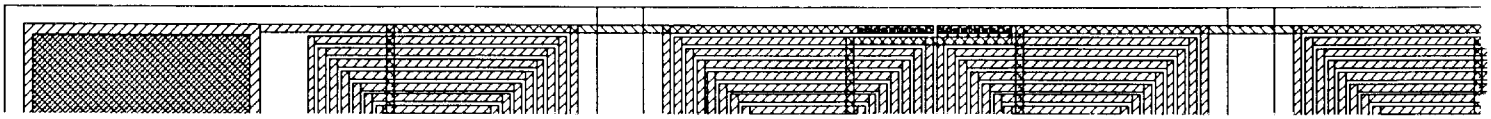
Design Name	Silicon Area (Square mils)	Nominal Resistance (Ohms)
INTANT	1465	1907

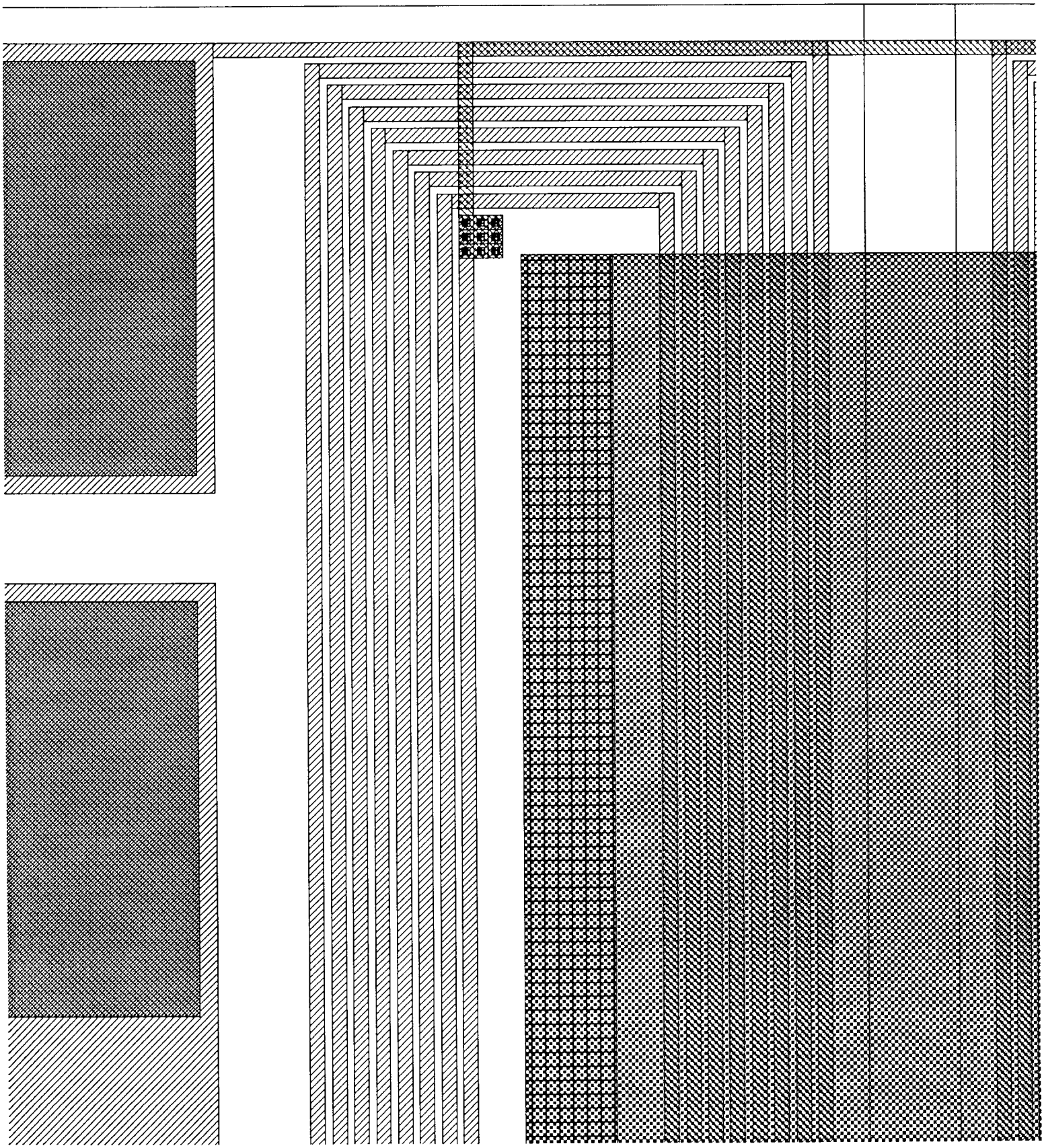

INTANT
WC-M1
PS-M1
PR-M1
PR-WC
M1-WC
M2-VI



INTANT







The process used for the INTANT device was developed specifically for this program. It is identical to the process used to manufacture the ARTCOIL design, which is described in the following section. A list of the process steps is given below, followed by a brief description of a typical processing run:

INTANT/ARTCOIL

Starting material is 2KÅ silicon nitride
Plating seed deposition 1KÅ permalloy
Core photo 1
Gold plate 1 - 2 microns
Gold plate thickness measurement
Core photo 2
Core plate 5 micron permalloy
Core plate thickness measurement
VIA deposition 7500 Å SOG/BSQ/silicon nitride
VIA deposition thickness measurement
M 1 deposition 5KÅ Al/Cu
M 1 photo
M 1 etch
VIA deposition 7500 Å silicon nitride
VIA deposition thickness measurement
VIA photo
VIA etch RIE
VIA etch thickness measurement
M 2 deposition 5KÅ Al/Cu
M 2 photo
M 2 etch wet etch
Electrical test contacts
WCON deposition 7500 Å silicon nitride
WCON deposition thickness measurement
WCON photo
WCON etch RIE
WCON etch thickness measurement
Plating seed deposition 1KÅ permalloy
Core photo 1
Gold plate 1 - 2 microns
Gold plate thickness measurement

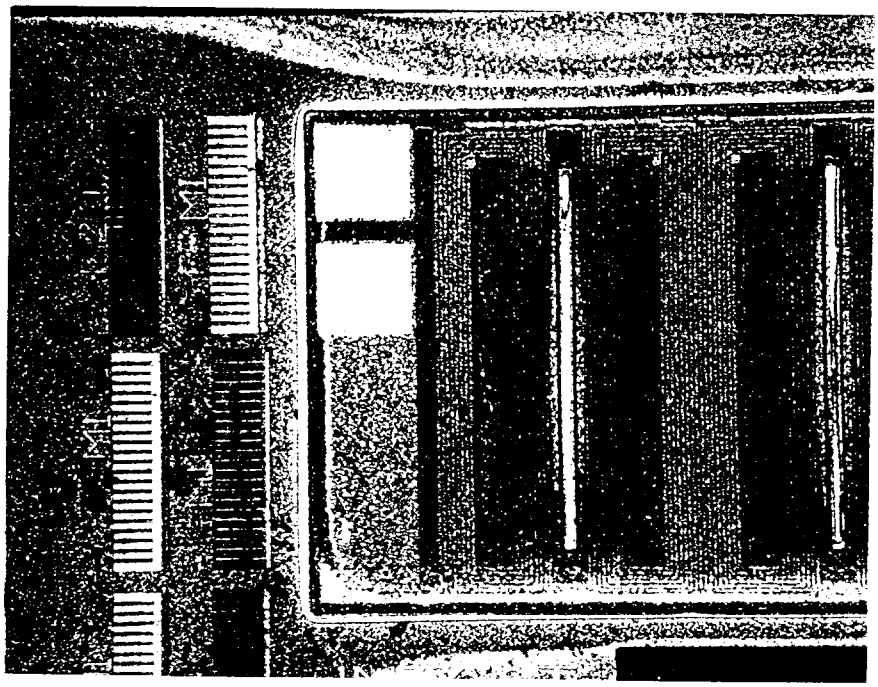
Core photo 2
Core plate 5 microns permalloy
Core plate thickness measurement
PSV photo
PSV etch
PSV etch thickness measurement
Electrical test

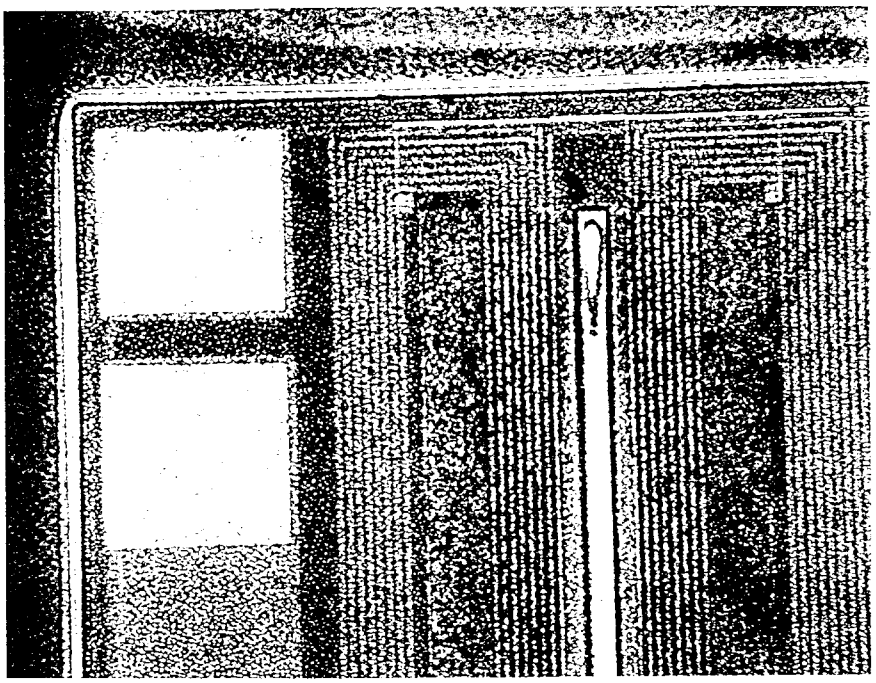
The process begins on a 4" silicon wafer covered with an insulating layer of 2000 Angstroms of silicon nitride. The first mask is used to pattern photoresist for the bottom core of the device. Gold is plated up through the photoresist to a thickness of about 1 micron(for adhesion purposes), then the wafer is remasked and permalloy(80% Ni, 20% Fe) is plated up to a thickness of about 5 microns to form the bottom core.

The next step is deposition of an insulating layer composed of Spin-On Glass(SOG), Bias-Sputtered Quartz(BSQ), and silicon nitride. On top of this layer, 5000 Angstroms of AlCu for use as Metal-1 is deposited. The second mask level is used to pattern and etch the Metal-1. Then, another 7500 Angstroms of silicon nitride is deposited. The VIA mask is used to pattern and etch contacts down to Metal-1, and 5000 Angstroms of AlCu is deposited to form the Metal-2 layer. The fourth mask layer is used to pattern and etch the Metal-2. The wafer is then taken out of the process line for contact resistance testing.

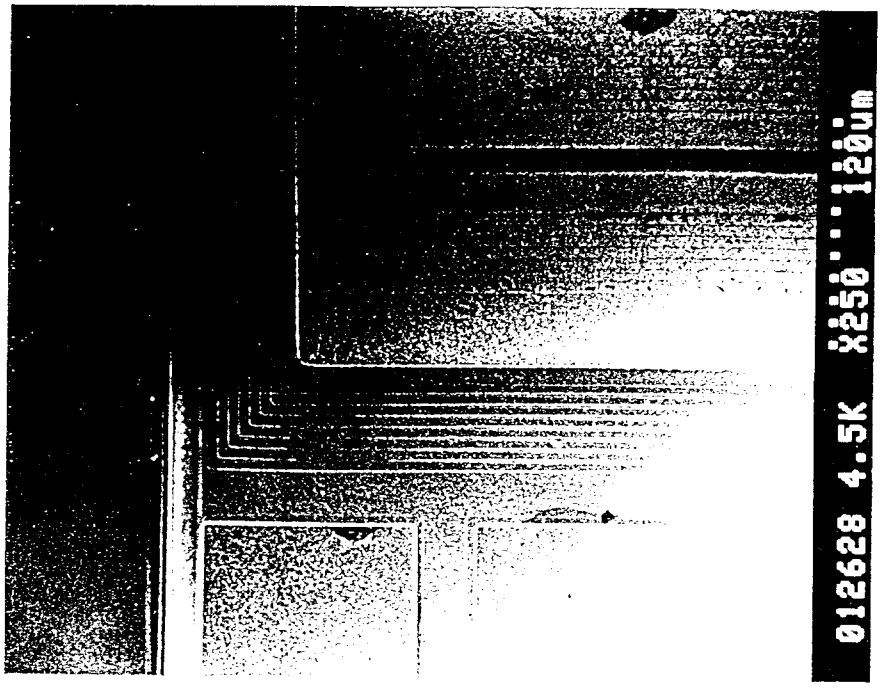
Following test, the another 7500 Angstroms of silicon nitride is deposited on the wafer, and the WCON mask layer is used to etch a hole in the nitride down to the bottom core structure. The next mask step defines the shape of the top core, and about 1 micron of gold is plated up through the photoresist to form this feature. The wafer is remasked, and 5 microns of permalloy is plated on top of the gold. Finally, the PSV mask is used to cut holes in the nitride down to the bonding pads so that the electrical connections to the device are available for test.

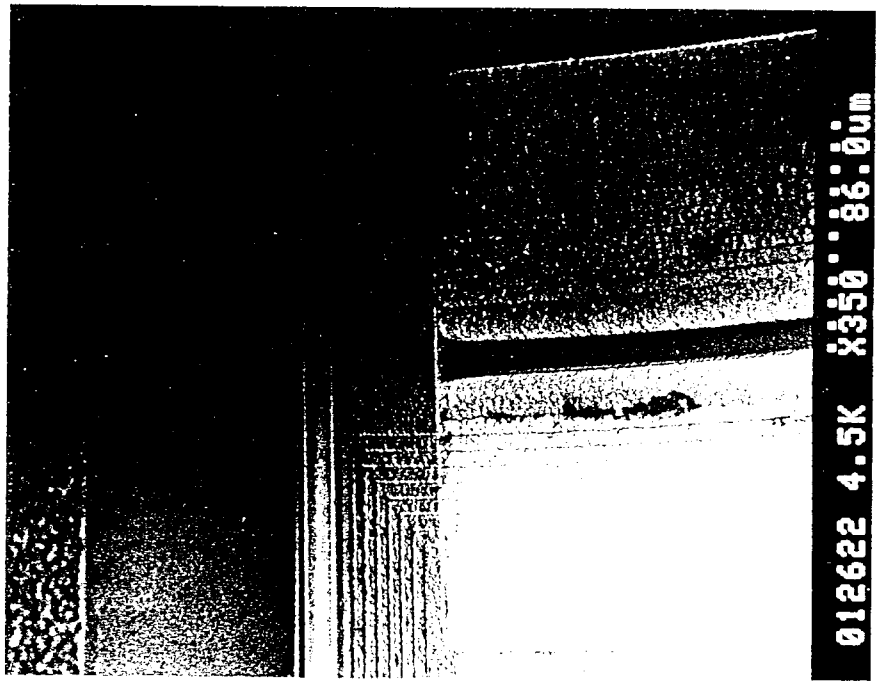
The photos on the following two pages show several view of the completed INTANT devices, taken with NVE's optical microscope.

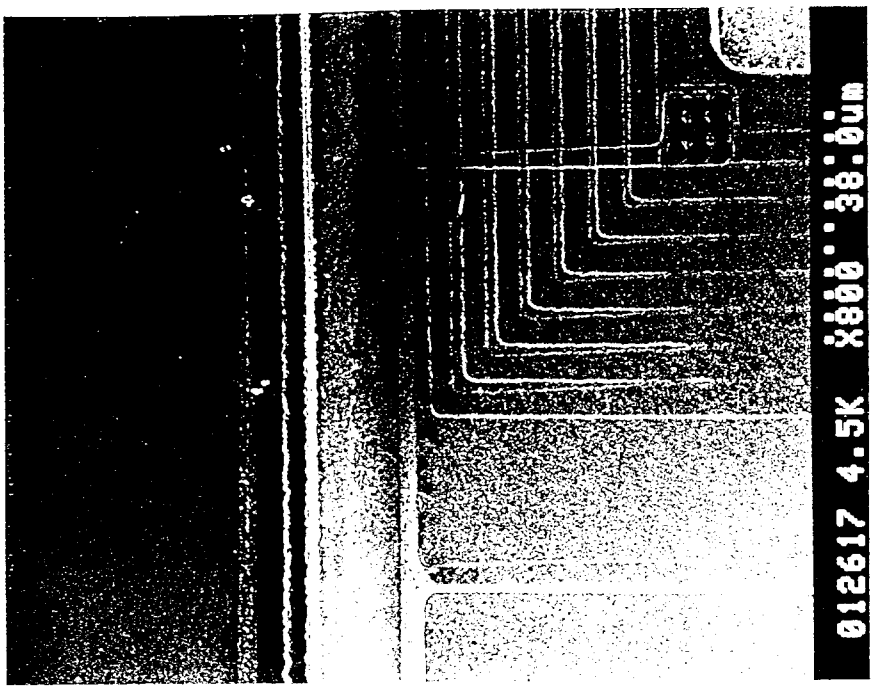


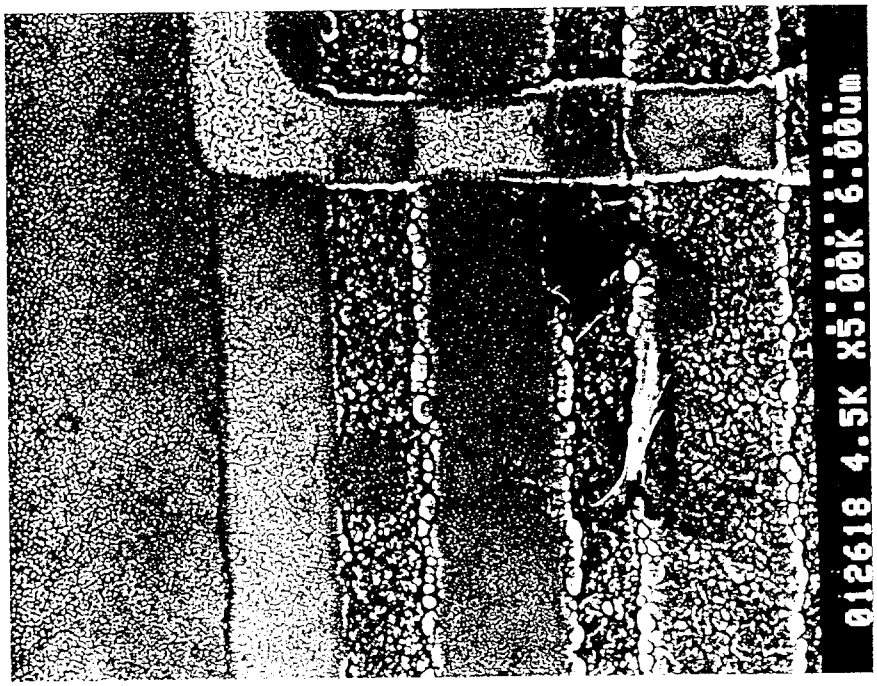


The yield of these devices was expected to be low because of the relatively thin metallization on top of the bottom core, and the large number of windings made from this metal. In fact, no testable devices were found on any of the wafers processed for this design. Every device exhibited shorting problems. After the failure analysis was performed on the PLTANT devices, the reason for this became clear. The PLTANT devices exhibited shorting problems with plated metal lines that had a 5 micron gap between them. The design rules used for Metal-1 and Metal-2 in the INTANT design specified minimum spaces of only 2 microns. This tolerance can be held without any problem on the surface of the wafer, but due to the focus and photoresist profile problems on top of the permalloy bottom core, these tolerances are not large enough. On the following two pages are electron microscope pictures taken of the INTANT design that clearly show the shorting problem.


012628 4.5K X250 120um


012622 4.5K X350 86.0um


012617 4.5K X800 38.0um


012618 4.5K X5.00K 6.00um

Increasing the minimum metal spacing requirement would fix the problems seen with this design; however, the reduced number of coils would probably make the device unusable for this application. NVE has devised an alternative approach to be tried in Phase II of this work. This approach is based on the method used by NVE's photolithography equipment to focus the camera. Currently, at several discrete points on the wafer, a laser beam is used to determine how far the surface of the wafer is from the camera. The camera in the GCA stepper is focused accordingly. Up until now, this area of the wafer has been clear of any structures, so that the laser bounces off the wafer substrate. NVE's idea is to alter the photomask design so that a permalloy core is plated in the areas where the laser is used to determine the camera range. This permalloy core would be outside of any functional device; its only purpose would be to duplicate the elevated features that the metal lines sit on. When it came time to focus the camera, the laser would find the range to the top of the permalloy core, and the camera would provide the proper focussed image. The details of this approach remain to be worked out, but an initial look at the stepper operation indicates that it would be feasible. Note that this approach does not necessarily provide benefits for the plated antenna (PLTANT) design, because in that case the windings have to be defined on top of the permalloy core *and* on the surface of the wafer itself.

As a result of this Phase I program, NVE has drawn the following conclusions about the integrated antenna (INTANT) design:

1. Electrical simulations showed that this design would be functionally adequate for use as an on-chip antenna, if it could be manufactured. It was not, however, as promising as the plated antenna design.
2. Processing problems prevented any devices from being tested for proper operation.
3. The primary processing problem has been identified, and a fix for the problem has been proposed. More processing is required to determine if this fix will resolve the problem.

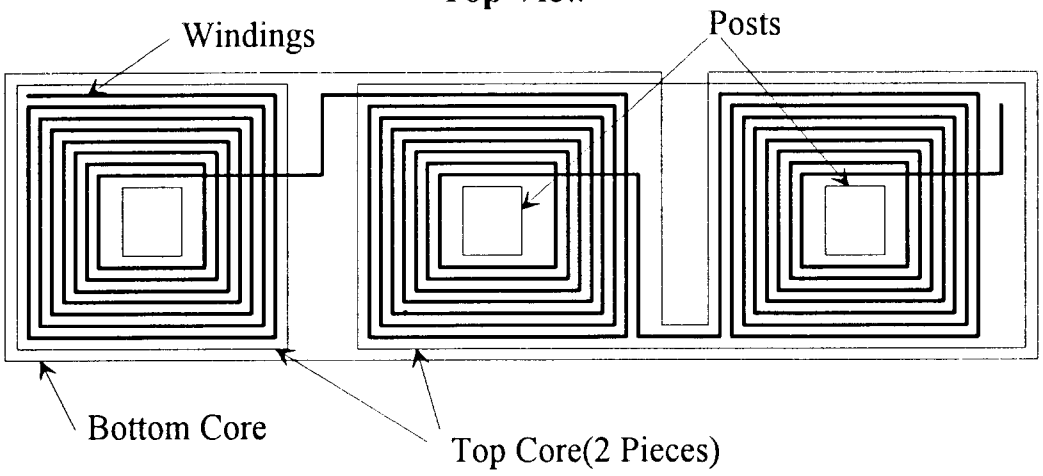
4. ARTCOIL - This is the other antenna design invented after the Phase I proposal was already submitted. It is similar in construction to the previous (INTANT) design, and in fact the processing is identical. However, the number of turns is significantly increased using this design, by covering the Metal-1 pattern with a duplicate pattern in Metal-2. This essentially doubles the number of turns, providing a very high mutual inductance. The drawback of this approach is the large number of turns; this leads to a very high winding resistance. As in the INTANT, this high winding resistance limits the Q multiplication effect available with this design.

This design was evaluated in detail for the purposes of electrical simulation at the beginning of the program. The resistance of the windings was determined to be about 12.3 Kohms, but the self inductance was 3 milliHenrys, which is the largest self inductance of any of the antennae. However, during the HSPICE simulations with the design, a basic flaw was discovered in this design. There is a frequency level, referred to as f_c, where the size of the tank capacitor required for resonant circuit operation is exceeded by the parasitic capacitance of the device itself. When the frequency of operation falls above this point, a tuned circuit is no longer possible. It was discovered during the HSPICE simulations that f_c was below the minimum frequency required for chip operation; in other words, in order to generate the voltage required by the chip circuitry, the RLC resonant circuit had to be operated in an out of tune state which is not desirable.

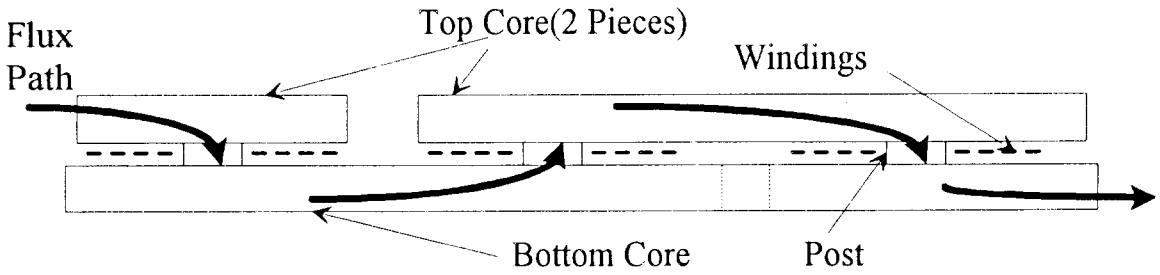
Up to this point, NVE had determined that reproducing a 5 volt supply on the chip was desirable; however, a lower voltage circuit was a possibility. NVE considered abandoning the ARTCOIL design briefly, but since the masks had already been ordered and the process used to make the ARTCOIL was the same as the INTANT process, no additional costs would be incurred by running the mask set through the process line and testing the ARTCOIL at the end of processing. Work on the ARTCOIL therefore proceeded on schedule, with the hope that either the parasitic capacitance calculations performed for this design were in error, or that the circuitry could be made to function at a lower voltage.

Top and side view drawings that show the basic construction of this device are shown on the following page:

Top View



Side View

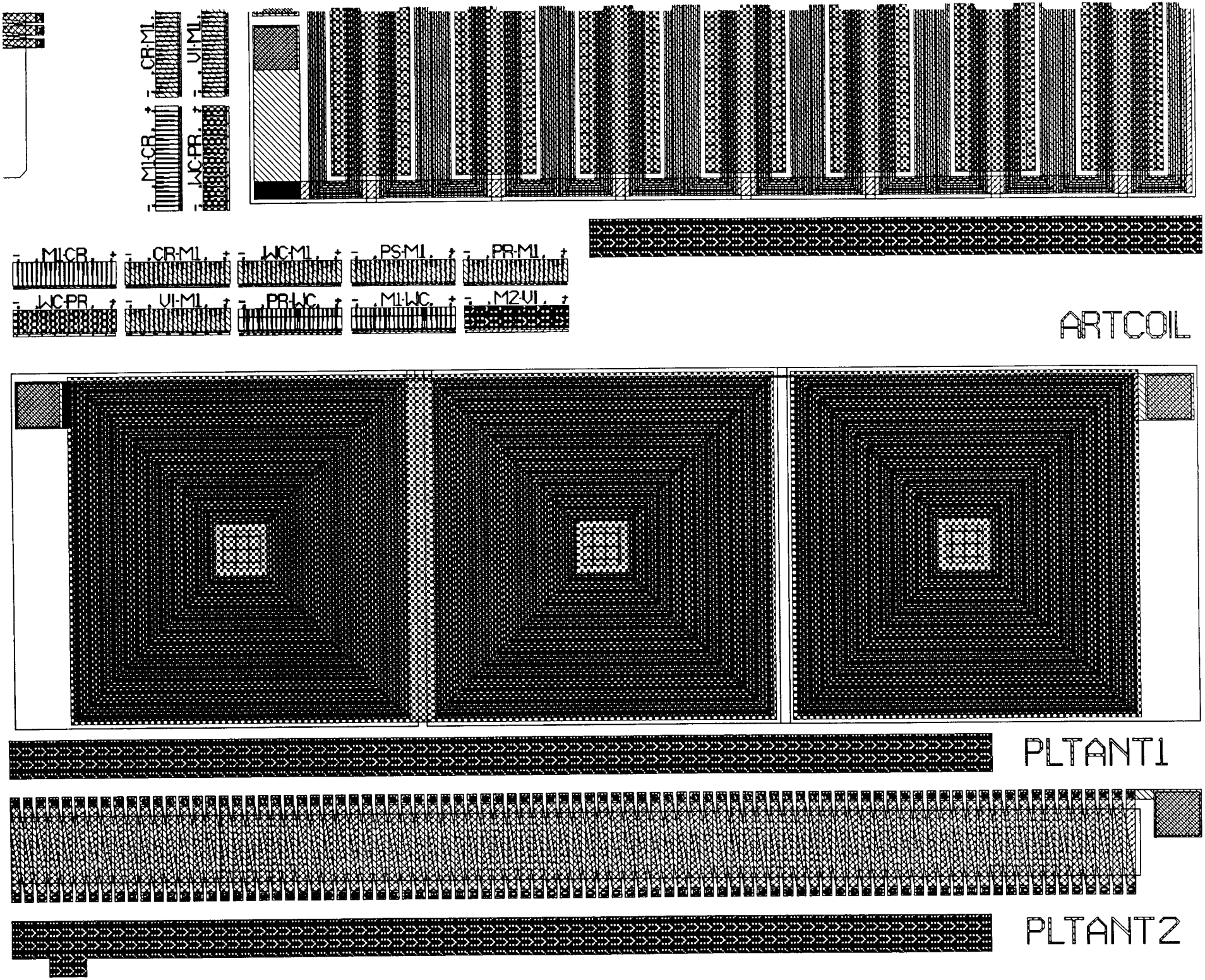


The flux path shown cuts through the windings by travelling through the post in their center. The post is not actually a separately deposited structure, but part of the top core. The side view shows that this design is similar in functionality to the INTANT device.

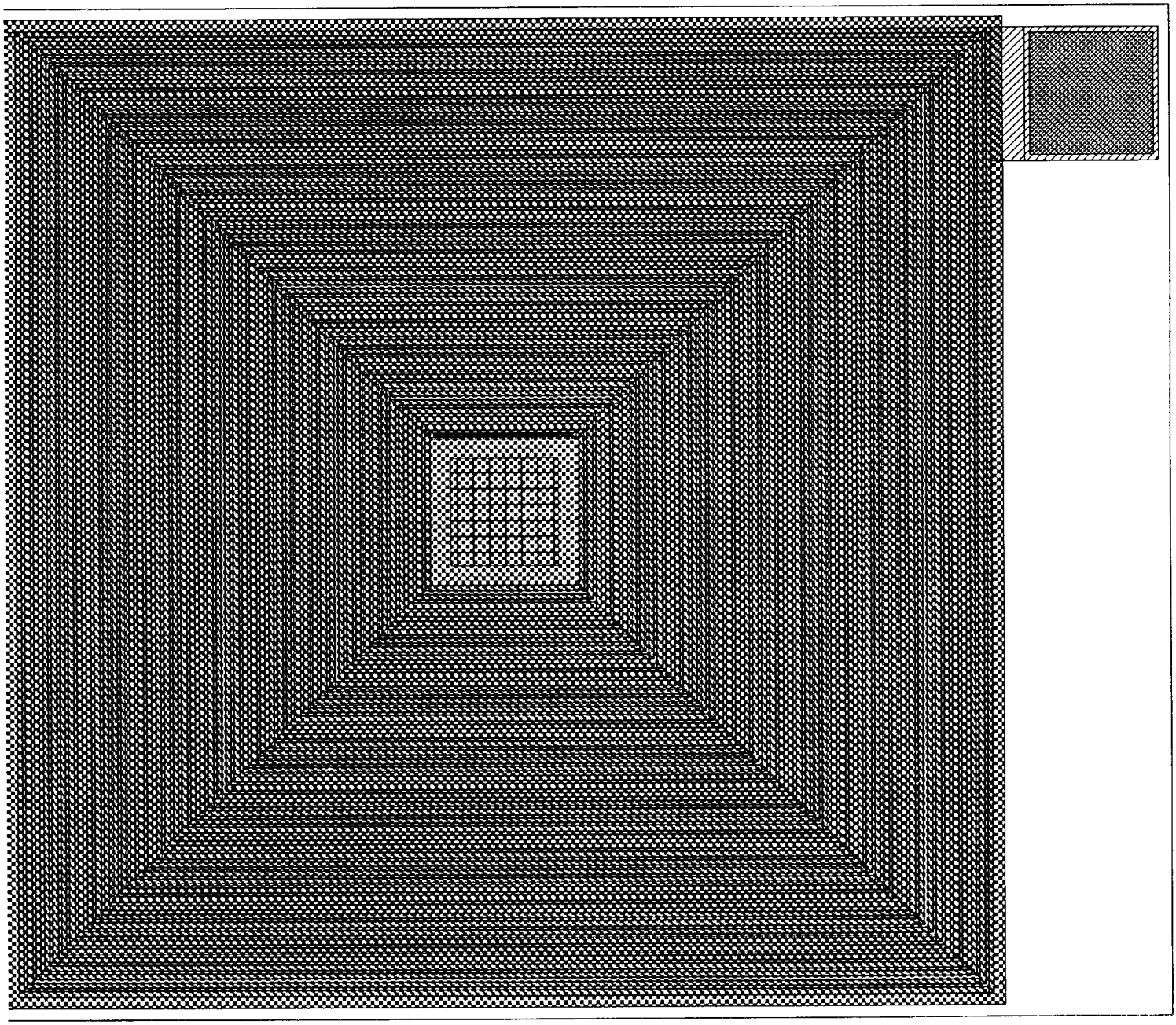
Since the ARTCOIL is such a large device, only one was laid out on the mask set. Like the INTANT design, the bonding pads for the ends of the windings are positioned on top of the bottom core, and wire bonds would be required to connect the windings to any circuitry on the semiconductor substrate. The area and electrical design characteristics of the ARTCOIL are given in the table below:

Design Name	Silicon Area (Square mils)	Nominal Resistance (Ohms)
ARTCOIL	2895	12,330

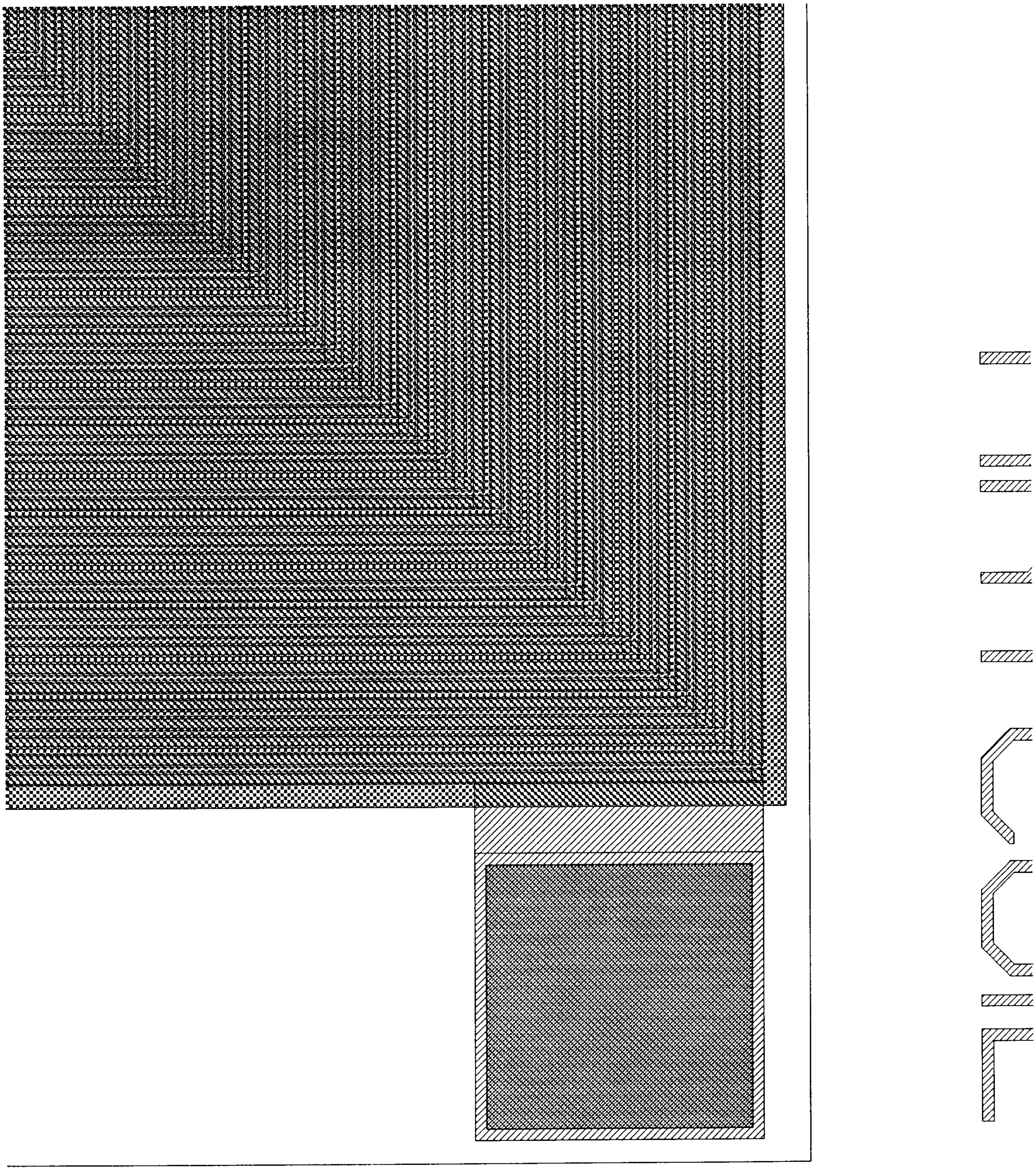
Plots of the ARTCOIL design are shown on the following three pages.


CR-M1
VI-M1
M1-CB
WC-PR
M1-CB
CR-M1
WC-M1
PS-M1
PR-M1
WC-PR
VI-M1
PR-WC
M1-WC
M2-VI
ARTCOIL
PLTANT1
PLTANT2

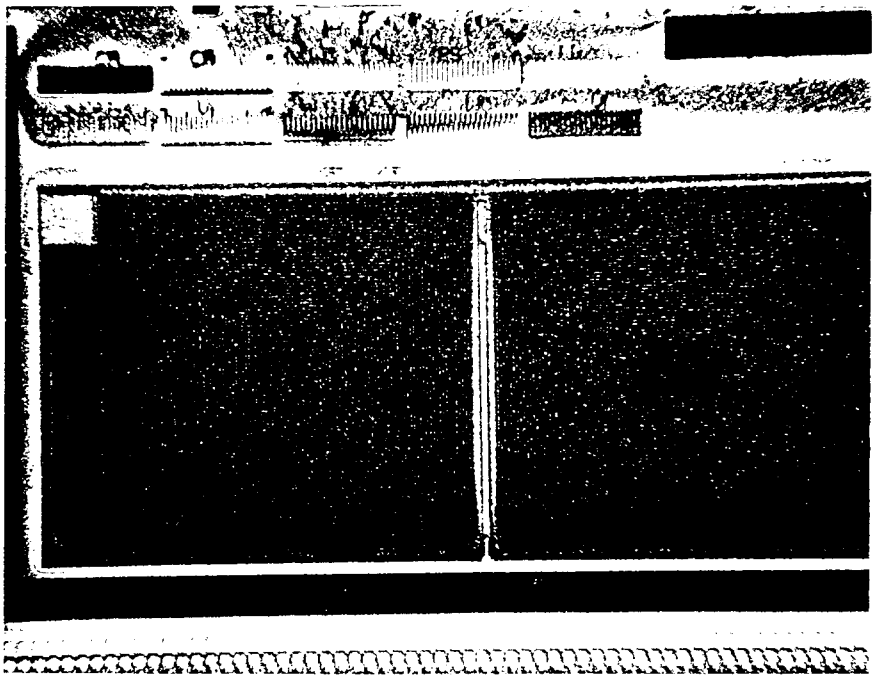
ARTCOIL

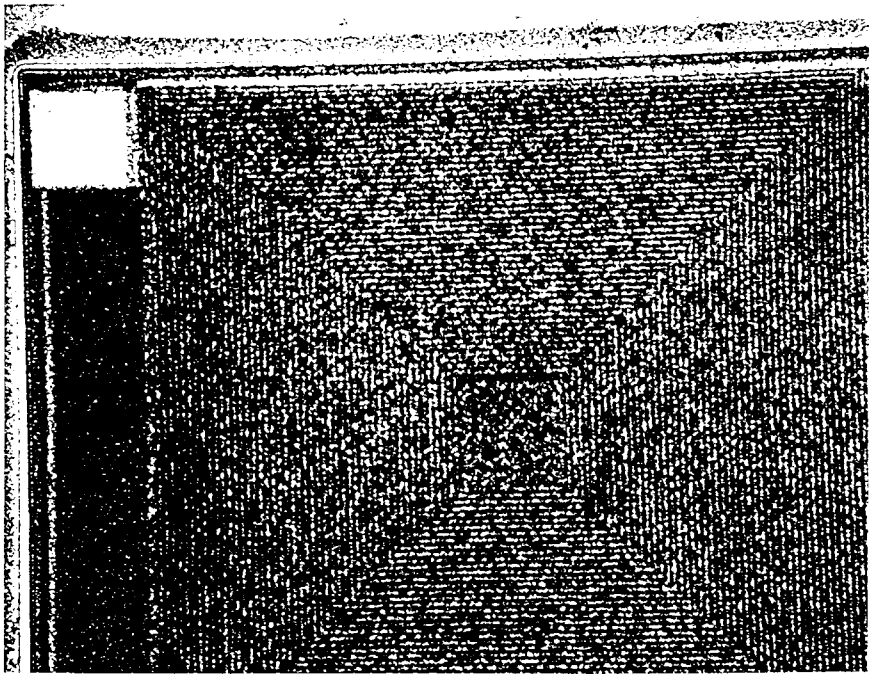


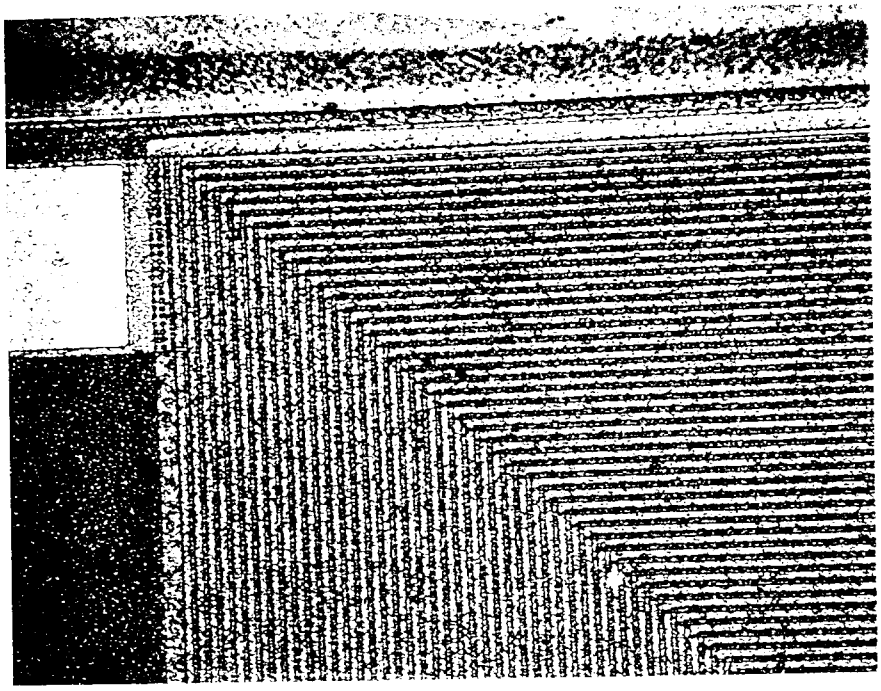
PLTANT1



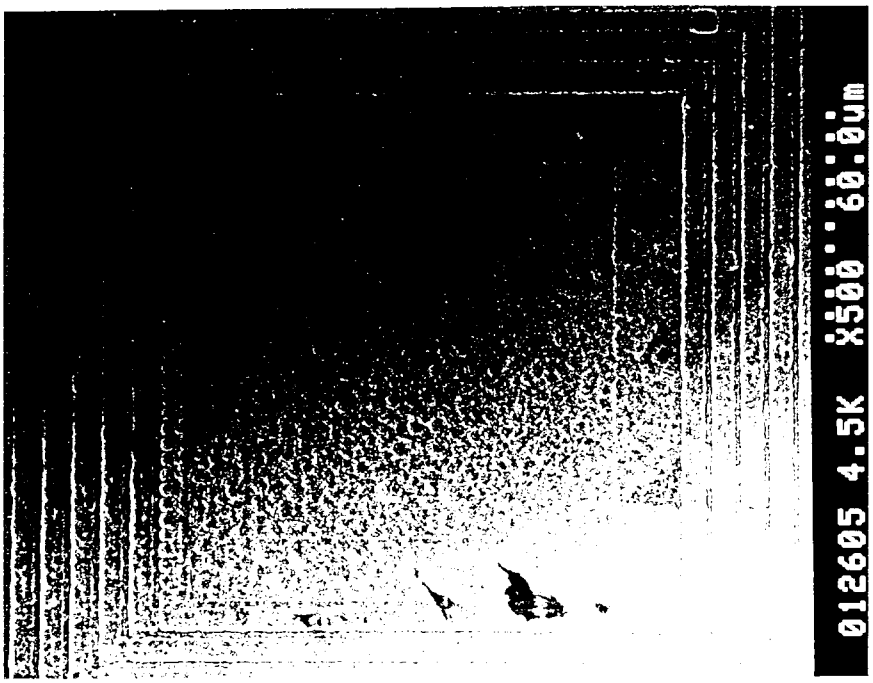
The process used for the ARTCOIL devices is identical to the process described in the previous section for the INTANT devices. The photos below and on the following page are optical photomicrographs of the completed ARTCOIL device, taken at NVE's facility.

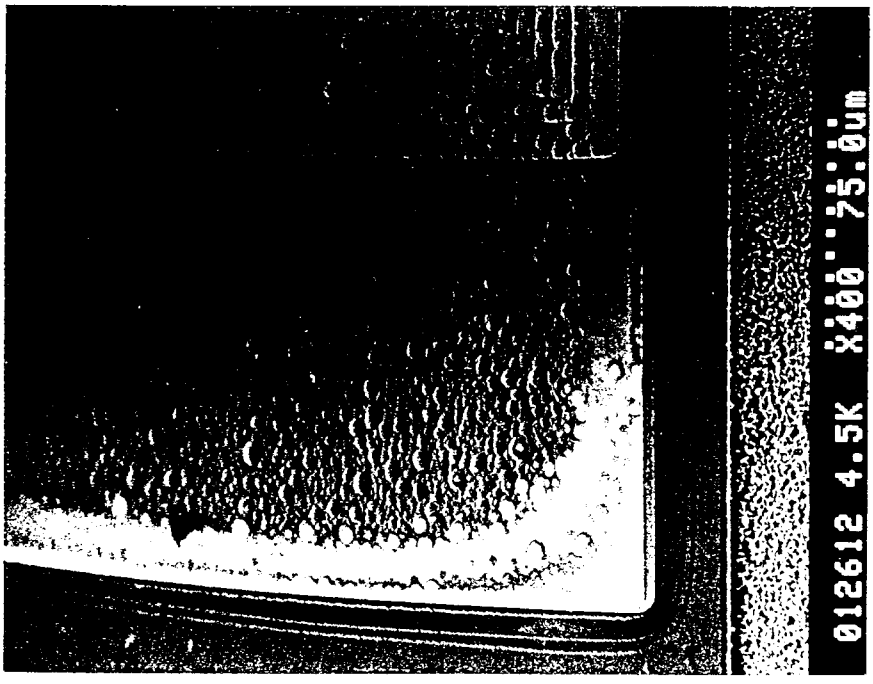


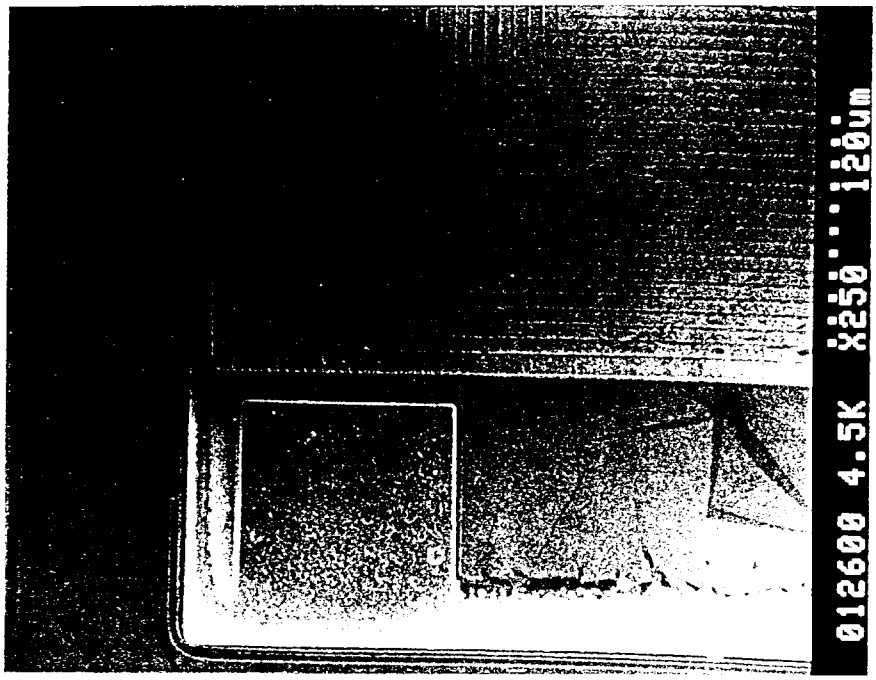


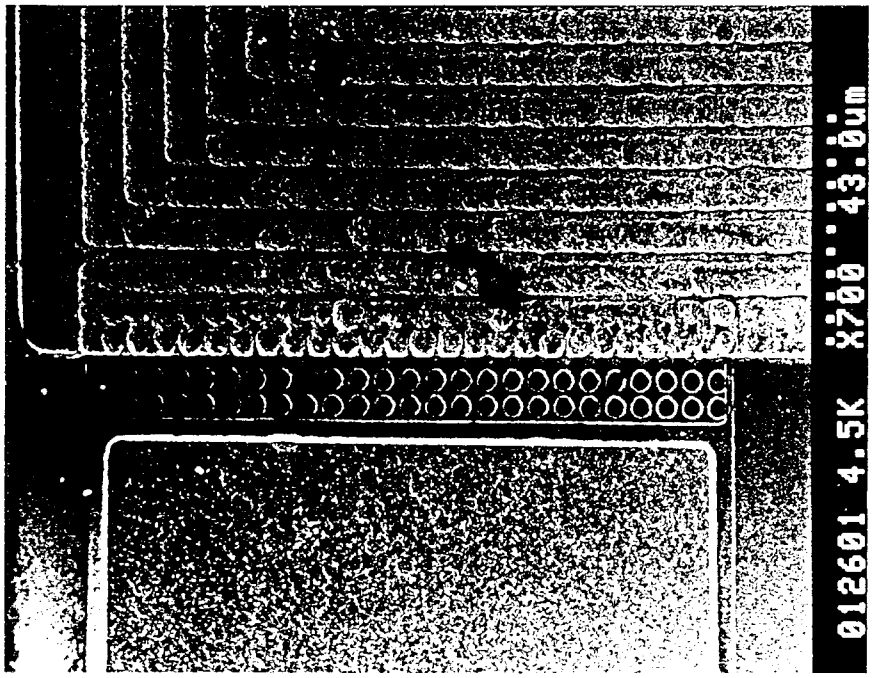


As with the INTANT devices, the ARTCOIL devices all exhibited shorting problems; no testable devices were found on the wafers. The reasons for these shorts are the same as mentioned in the previous section. Since the winding structure for the ARTCOIL is more complex than that of the INTANT, the shorting problem appeared even more severe. The electron microscope photos on the following two pages illustrate some good and bad sections of the device. Notice in the first two photographs, which show relatively good areas, the metal lines are still ballooned and scalloped due to the out of focus condition on top of the bottom core.


012605 4.5K X500 60.0um


012612 4.5K X400 75.0um


012600 4.5K X250 120um


012601 4.5K X700 43.0um

The same process change described in the INTANT section, involving creating a plated pedestal on the wafer for the stepper camera to focus on, would likely fix the shorting problems seen on this design as well.

As a result of this Phase I work, NVE has drawn the following conclusions about the ARTCOIL design:

1. Detailed electrical analysis and HSPICE simulations of this design indicate that it would not function as an adequate on-chip antenna, unless the winding resistance was decreased or the chip's voltage requirements were lowered.
2. Processing problems prevented any of the ARTCOILS from being tested to verify the simulations.
3. The processing modification proposed for the INTANT design would also fix the ARTCOIL design, if the modification is successful.

General Conclusions Regarding On-Chip Inductor Research - Given the difficulty involved in developing two completely new IC processes, NVE considers the results of this part of the program very encouraging. It was our hope at the beginning of this work that a functioning antenna would be the result, and since this didn't happen, we are obviously disappointed. However, the thorough failure analysis done on the antenna wafers clearly showed the extent of the problems, and NVE process personnel are very confident that another pass will result in good plated antenna (PLTANT) devices. In addition, the INTANT devices should function provided the proposed solution to the focussing problem can be implemented.

NVE will continue with the process development, as internal R&D funding permits.

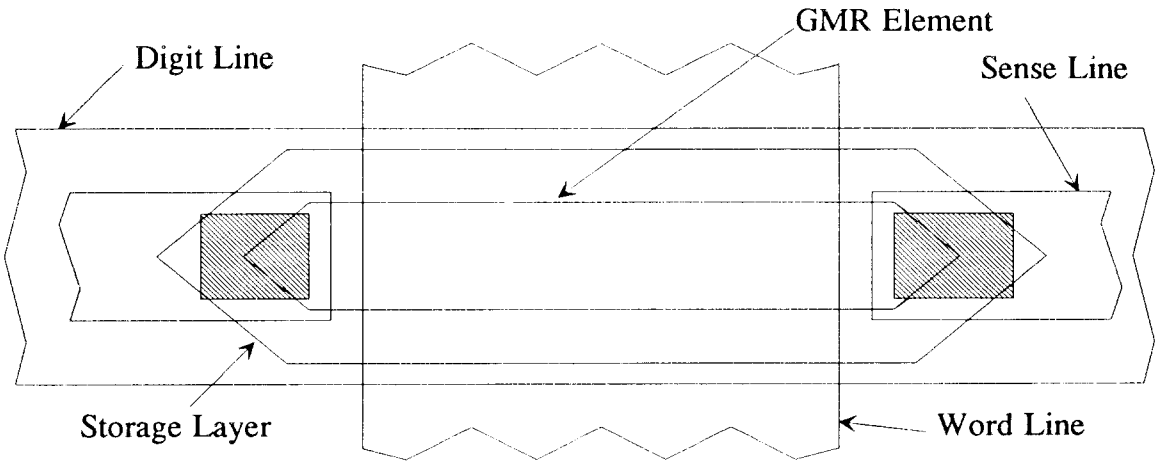
Low Power MRAM Memory Cell - The memory cell development completed during this program conclusively shows that a writable RFID chip based on MRAM technology is feasible. The MRAM cells developed for use in this application provided a large, bipolar read signal with a read current requirement of less than 10 mA. A larger current is required to write the memory cells; testing indicated that at least 30 mA is required. However, once this current turns on, the cells are written in 2 nanoseconds or less. This is the time it takes for the magnetization direction in the storage film to switch. The power supply on the chip is able to supply this current for at least 20 nanoseconds before the on-chip voltage drops to unusable levels, so writing the memory cells is not a problem. Typically, the circuit would be designed so that the write current remained on for only 5 or 6 nanoseconds.

The memory cells use three currents: sense line current, word line current, and torque or digit line current. In order to select a specific memory cell in the array, a current steering scheme is employed in the circuitry so the current can be shared or recycled by all three lines. In this way, no unnecessary power is lost. Two drawings of the construction of a typical memory cell are shown on the following page.

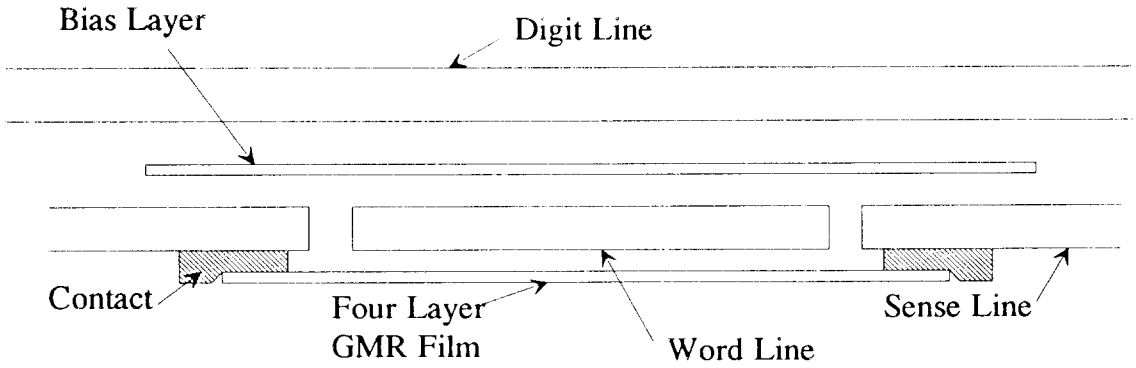
The mask set used for this program contains a total of 30 different types of memory cells for evaluation. These memory cells have varying widths of the different lines, varying lengths of the sensing element and the storage element, and different end shapes(the end shapes are particularly critical, because the magnetic fields in the memory cells will tend to reverse themselves if the ends are not properly defined). The optimum currents used to generate the magnetic fields that read and write the memory cells will vary slightly from design to design; however, in order to expedite the testing process, the requirements for a typical memory cell were determined, and then used for evaluating the remainder of the devices.

Materials used for the construction of these memory cells are listed in the table below:

Digit or Torque Line	98% Al, 2% Cu
Word Line	98% Al, 2% Cu
Sense Line Interconnect	98% Al, 2% Cu
GMR Sensing Element	4 magnetic layers NiFeCo, 3 non-magnetic layers Cu
Storage Layer	NiFeCo



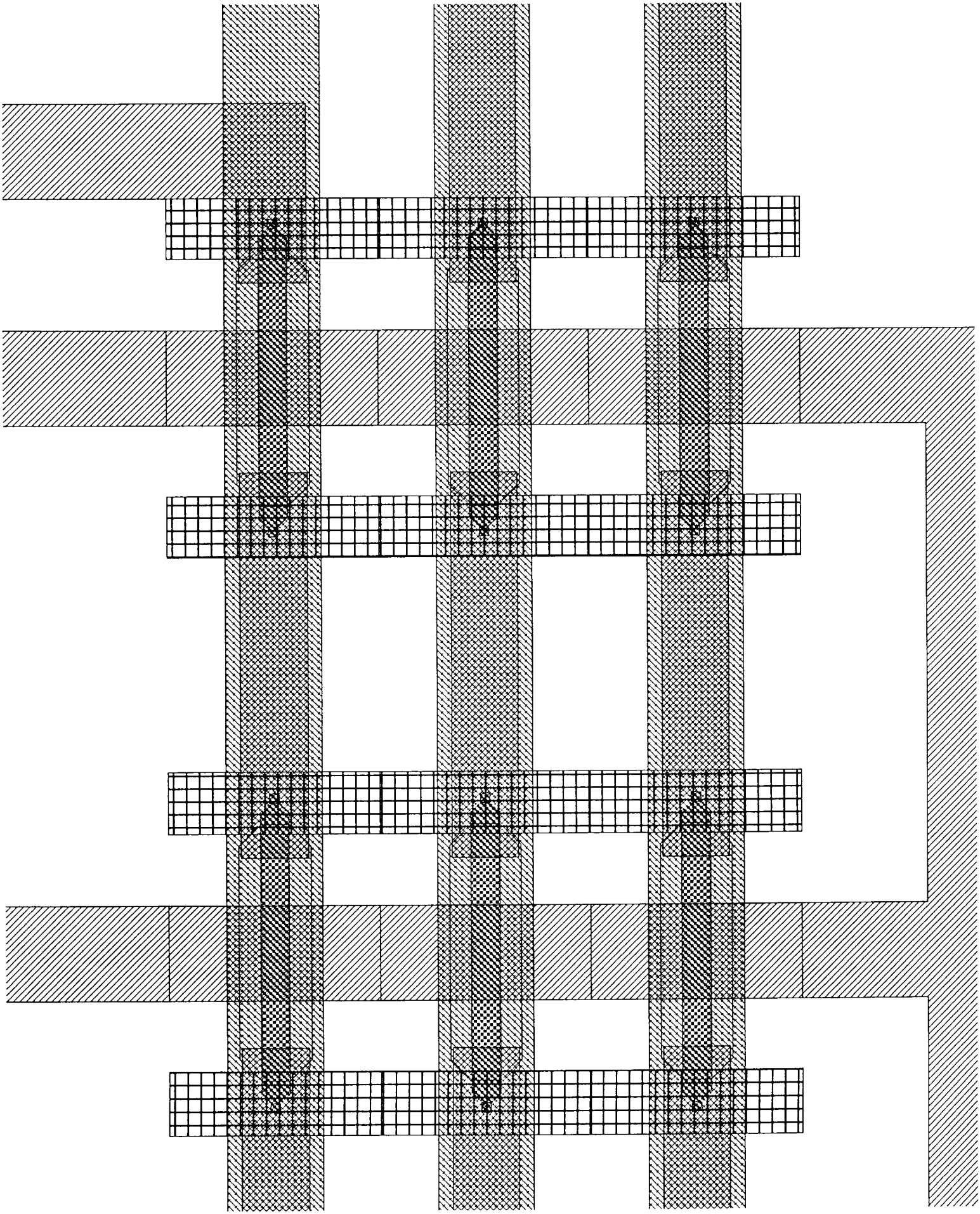
Top View of Memory Cell

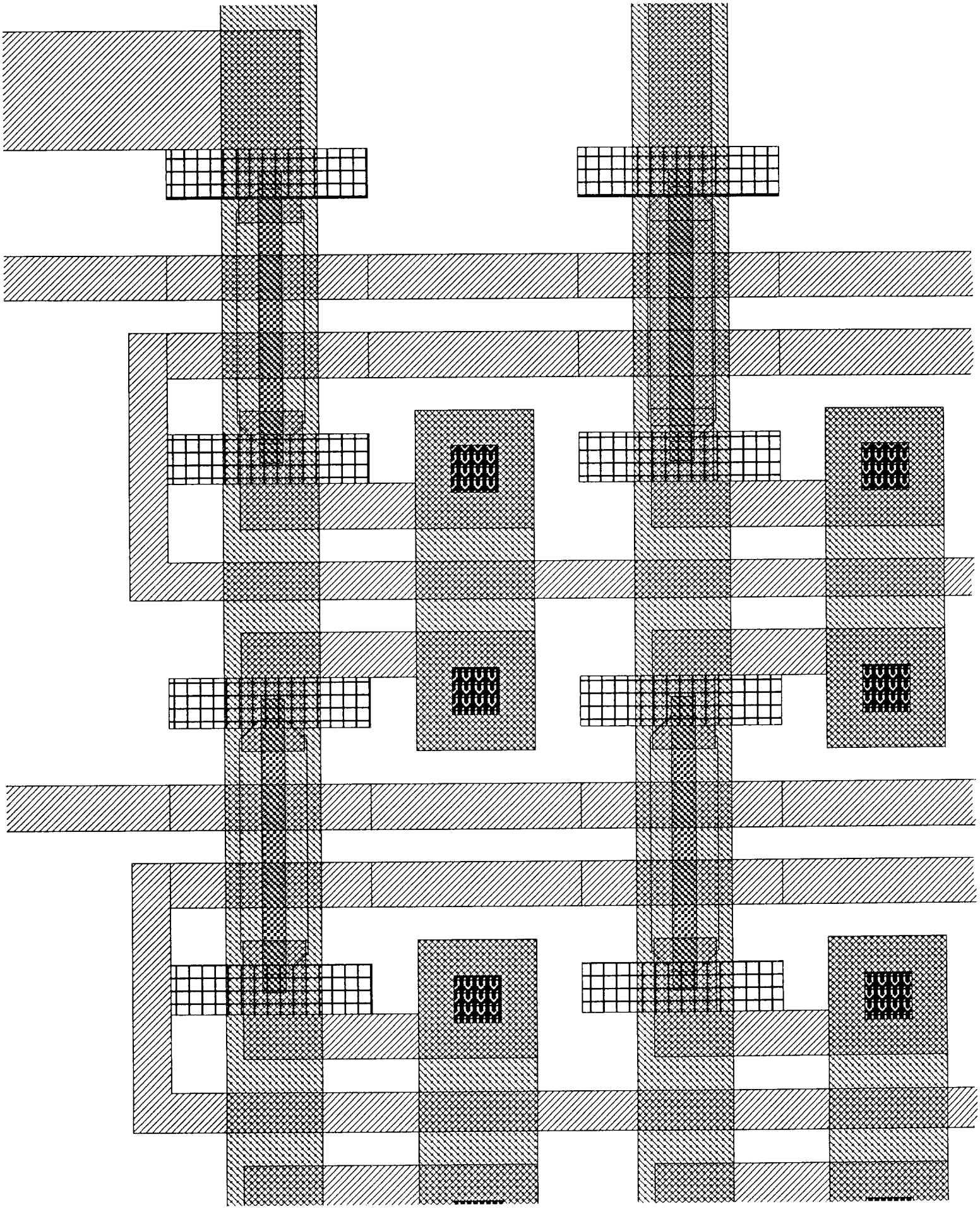


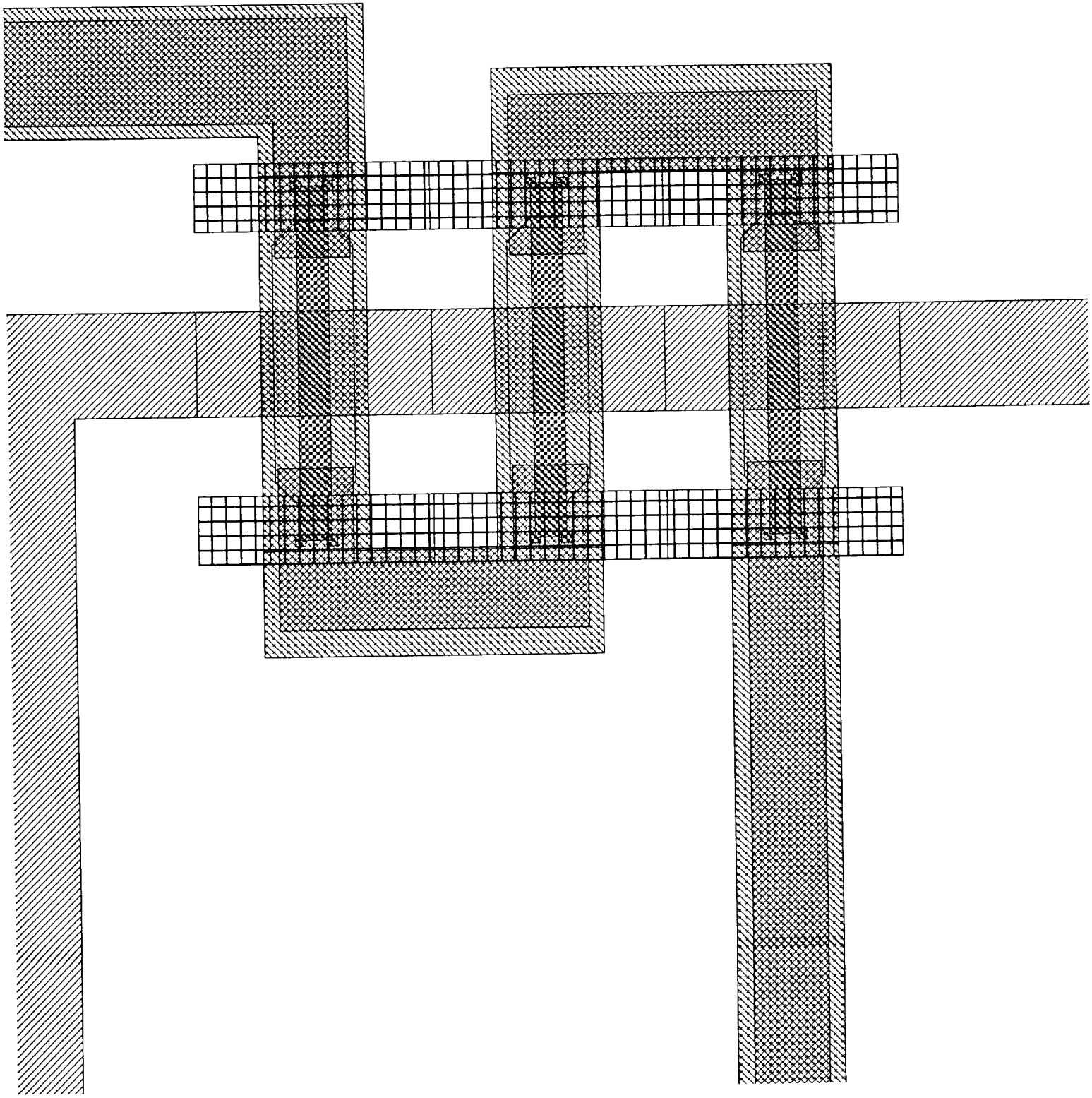
Cross Sectional View of Memory Cell

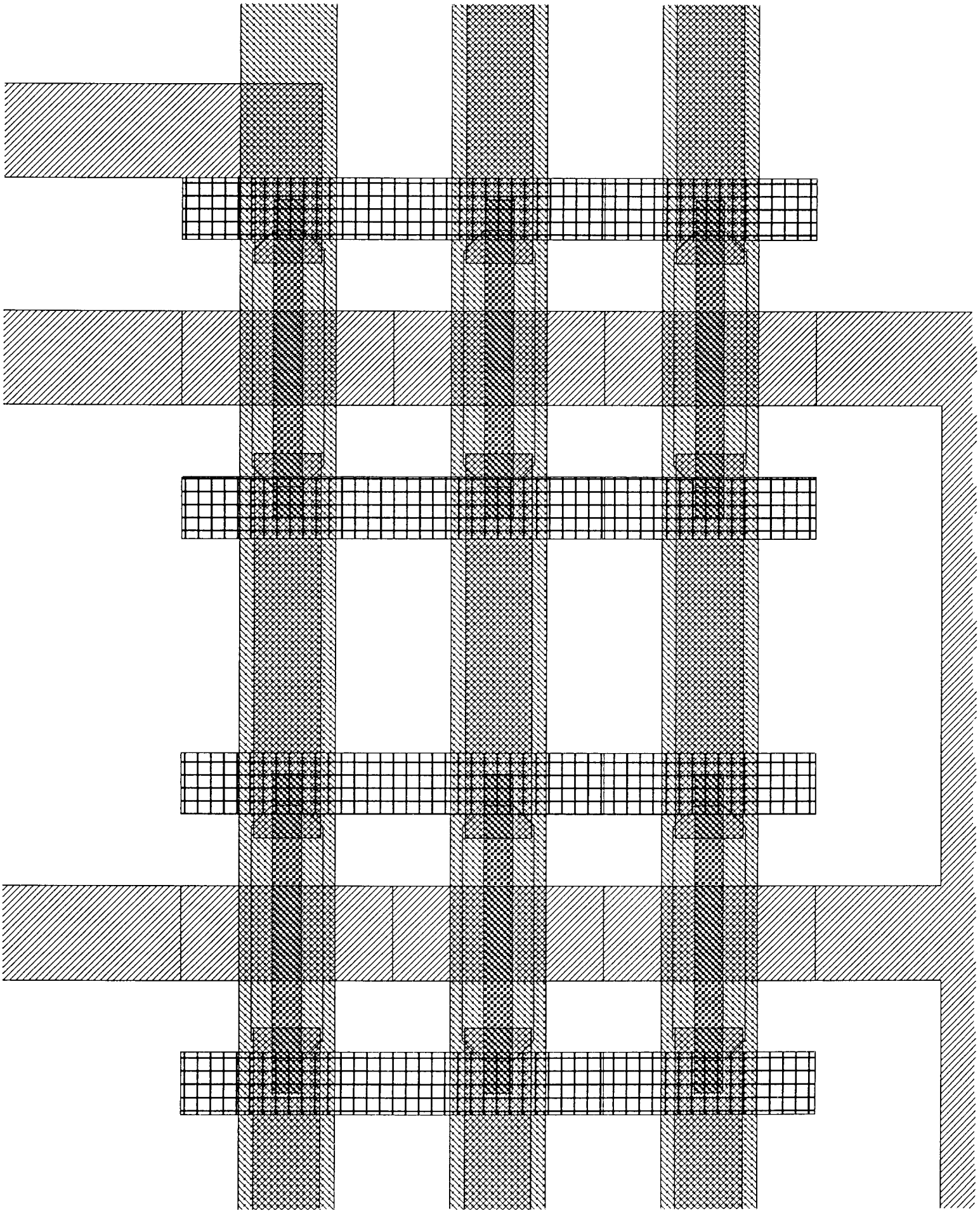
The digit line, word line, and sense line interconnect are standard 5000 Angstrom thick structures. The storage or bias layer is a thin film device, 200 Angstroms thick, and the four layer GMR sensing device is comprised of four magnetic thin films sandwiching 3 non-magnetic thin film interlayers. Total thickness of these layers is 200 Angstroms.

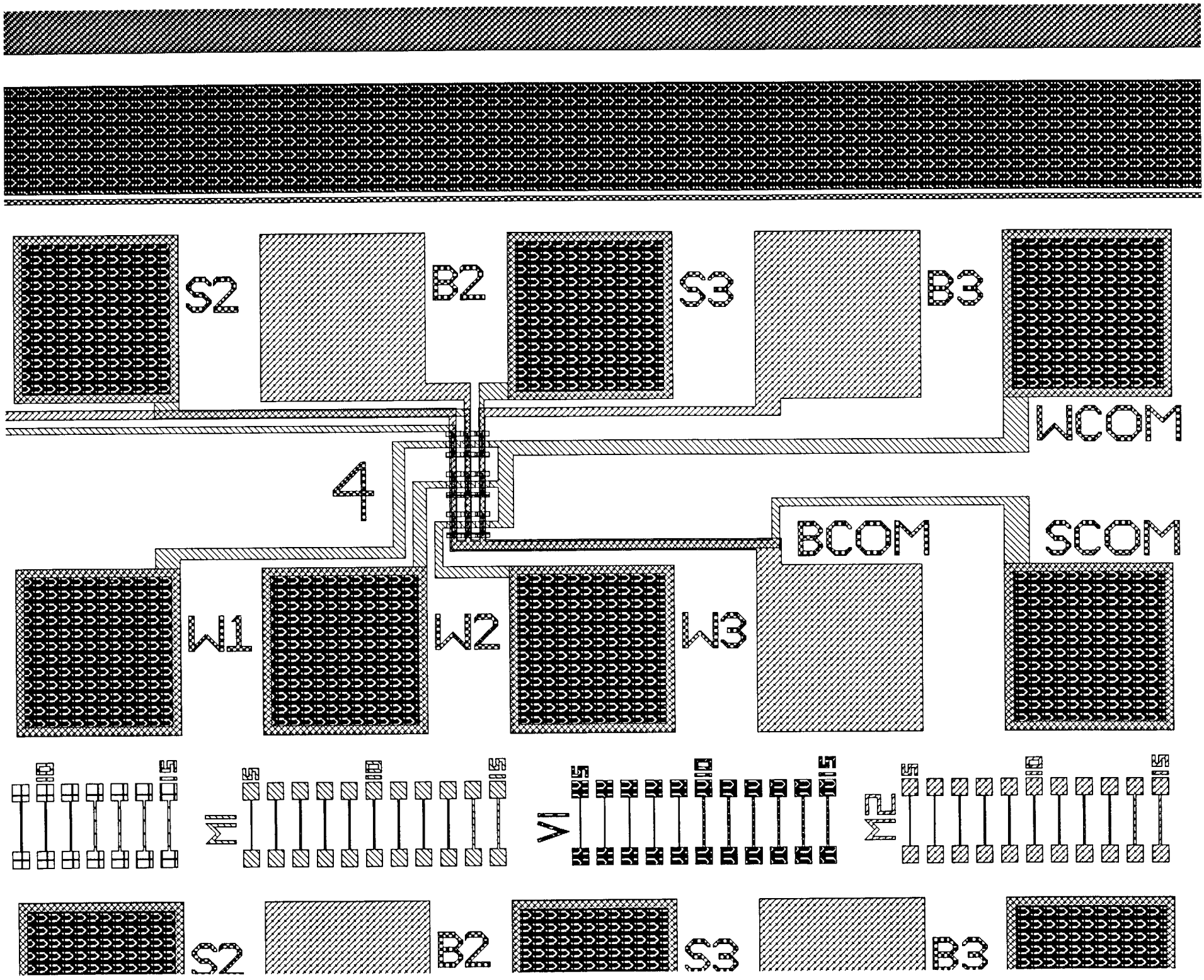
The plots on the following pages show four different types of memory cell layouts, one test array layout of these memory cells, and one plot of the entire test chip used for this program.

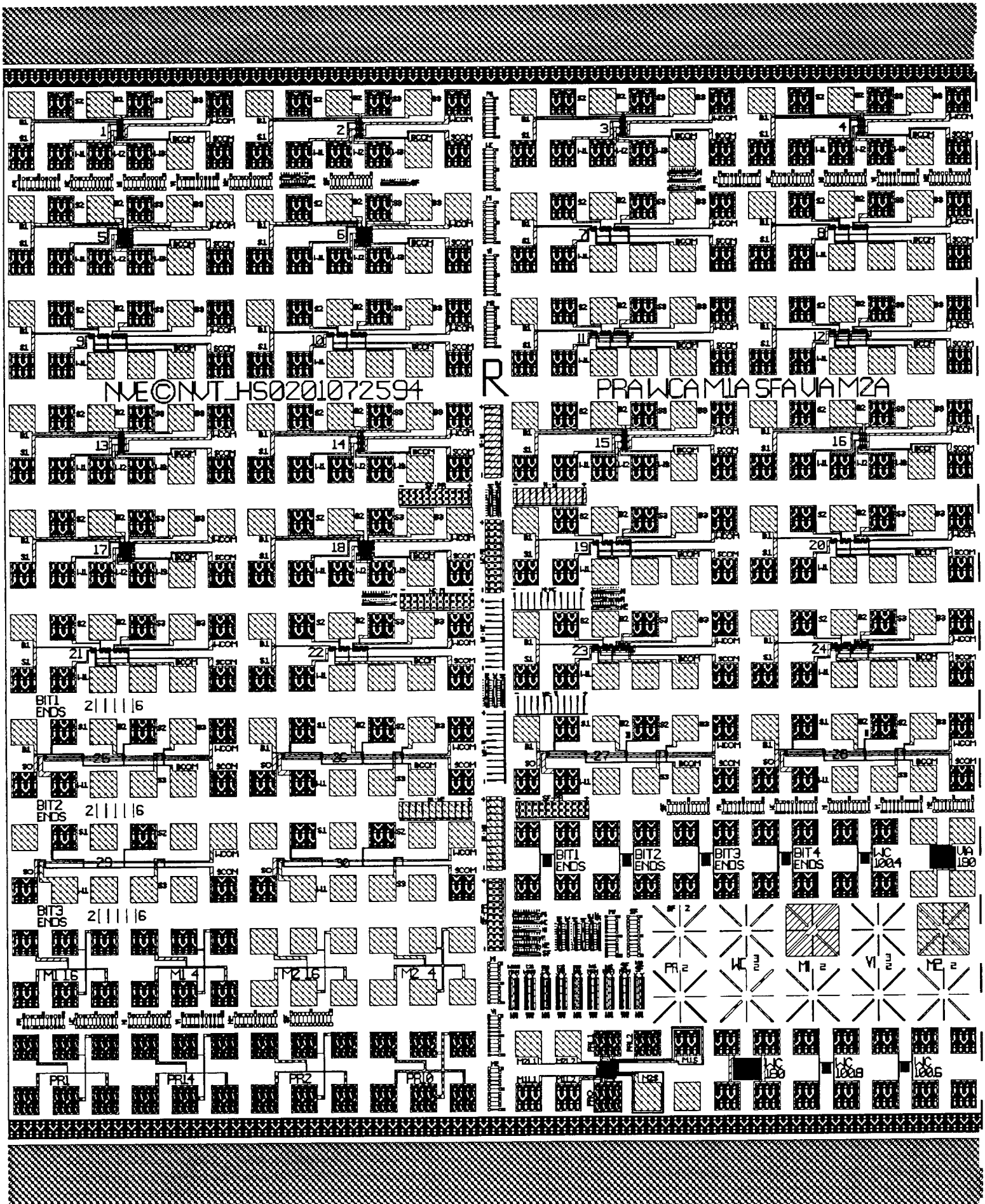









S2
B2
S3
B3
WCOM
4
BCOM
SCOM
W1
W2
W3
M1
V1
M2
S2
B2
S3
B3


NVE©NVT_HS0201072594
PRAWCAMIASFAVIAM2A
BIT1 ENDS 2||||6
BIT2 ENDS 2||||6
BIT3 ENDS 2||||6
BIT1 ENDS
BIT2 ENDS
BIT3 ENDS
BIT4 ENDS
M1 16
M1 4
M2 16
M2 4
PR1
PR14
PR2
PR10

The wafers that contained these memory cells went through processing without incident and were available for test at the end of the fourth month of this program. Testing on the devices showed that nearly all were fully functional(the ones that were not functional were traced to a layout error, where the sense lines had been left disconnected from ground). The testing showed that the memory designs functioned within the electrical design parameters, and would work in the RFID chip. However, NVE feels that various memory cell parameters could use improvement. In addition, there may be performance gains to be had by varying the memory cell geometries in different ways than was done with the first mask set.

Typical memory cells provided a bipolar read signal of +/- 1.2 mV; ganging several of these memory cells together increases the size of the read signal accordingly. Each memory cell on the test chip occupies an area in the array of 10μ X 10μ. A typical RFID chip uses 64 or 128 bits of memory; the area occupied by a 128 bit array of these MRAM memory cells is less than the area occupied by a typical bonding pad. Increasing the density of the memory array is not a challenge, because the arrays on the test chip were laid out with very wide spacing. NVE estimates that by increasing the density of the array, and increasing the number of memory cells for each logical bit to 8, a bipolar read signal of +/- 10mV can be obtained while the array remains as small or smaller than a typical 128 bit ROM array on RFID chips currently available.

Pertinent observations obtained from the testing procedure and relative to the design of the memory cells are described in the sections below:

1. Double Wrapped Word Line - This trick was tried on a number of the arrays for the purpose of increasing the current density over the memory cell. The idea is based on the principle that the current density, not the actual amount of current, determines the magnetic field in the proximity of a wire. Using smaller line widths, NVE wrapped the word line over the memory cell twice on these devices. Because of the process design rules, this geometry resulted in a word line area that was larger than the original word line by about 50%, so NVE expected current density and magnetic field to be increased by a factor of 1.5 on these designs. When testing, the current level was decreased by 1/3, but the results showed the memory cells did not work well in this way. The most likely explanation is that the process rules require a 2 micron space between the metal lines, and this 'dead' area over the memory cell caused the lackluster performance. A denser process than the one currently available at NVE may solve this problem, because the metal space could be reduced to 1 micron or less. This would result in a smaller

'dead' area, and the fringing fields from the metal lines would be stronger in the dead area because the metal lines would be closer together. NVE is upgrading its process facility in 1995, and suitable spacing may be available in our fab by the end of the year.

2. Bit End Shape - This has been a critical area for proper memory cell performance in the past, so a variety of different shapes were tried on this mask set to optimize the design. However, no significant differences between the designs were found during the test procedure. It is possible that the bit design that used the storage element is not sensitive to the shape of the end. It is also possible that since the GMR element in the sense line is not the memory information storage part of the memory cell, that the shape of the ends are not critical. In terms of the storage film itself, a single end design was used for all the devices, while the width of the device was varied. Disturb pulses placed on the digit, word, or sense lines tended to degrade the read signal size of the memory cells tested during this program. This may have something to do with the shape of the storage film ends. NVE feels that a mask redesign with varying types of storage film ends would be a worthwhile experiment.

3. Operating Currents - Obviously, on a device such as an RFID chip where the power supply is not inherently stable, the lower the power dissipation, the better. The memory cells designed for this program had a calculated current requirement of 40 mA maximum during the write cycle. However, in testing the optimum current was found to be 55 mA. This is an indication that the magnetic fields in the storage film were too difficult to switch. The storage film essentially acts as a bar magnet whose polarity switches when the magnetic field from the digit line and the word line is applied. A 'weaker' bar magnet would switch polarity with lower applied fields, making lower currents feasible. A redesign of the storage film ends, as described in the previous section, may provide this property; alternatively, the film thickness or composition could be varied.

Even with the high currents required to write these memory cells the RFID tag concept is feasible, because the storage films switch polarities in 2 nanoseconds or less; the energy required for a write operation is therefore extremely low. However, the lower the current required the better, so decreasing the current requirement of these memory cells would be a worthwhile pursuit in Phase II.

The next four pages show plots of typical memory cell outputs.

Front Panel

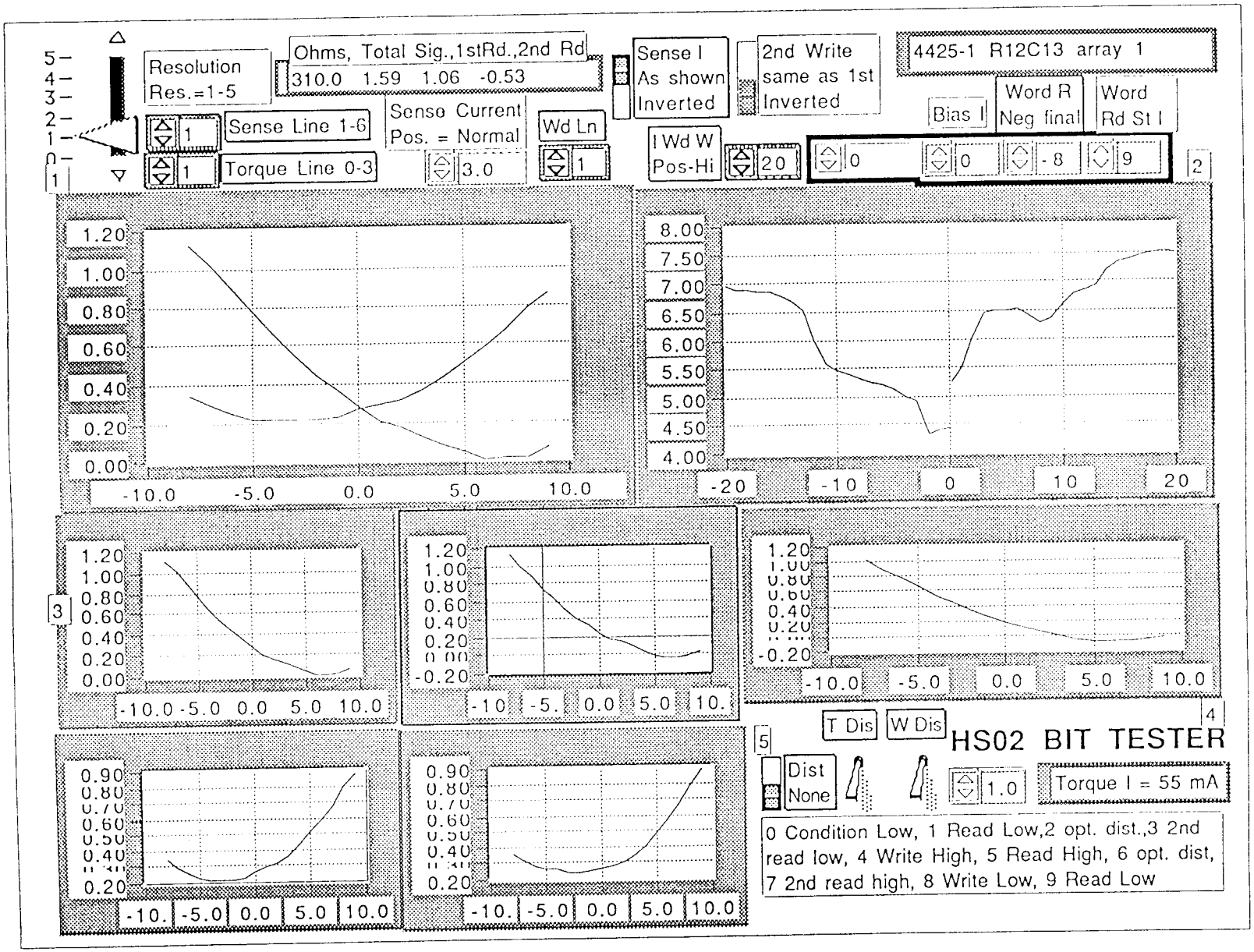


Fig. 3

Front Panel

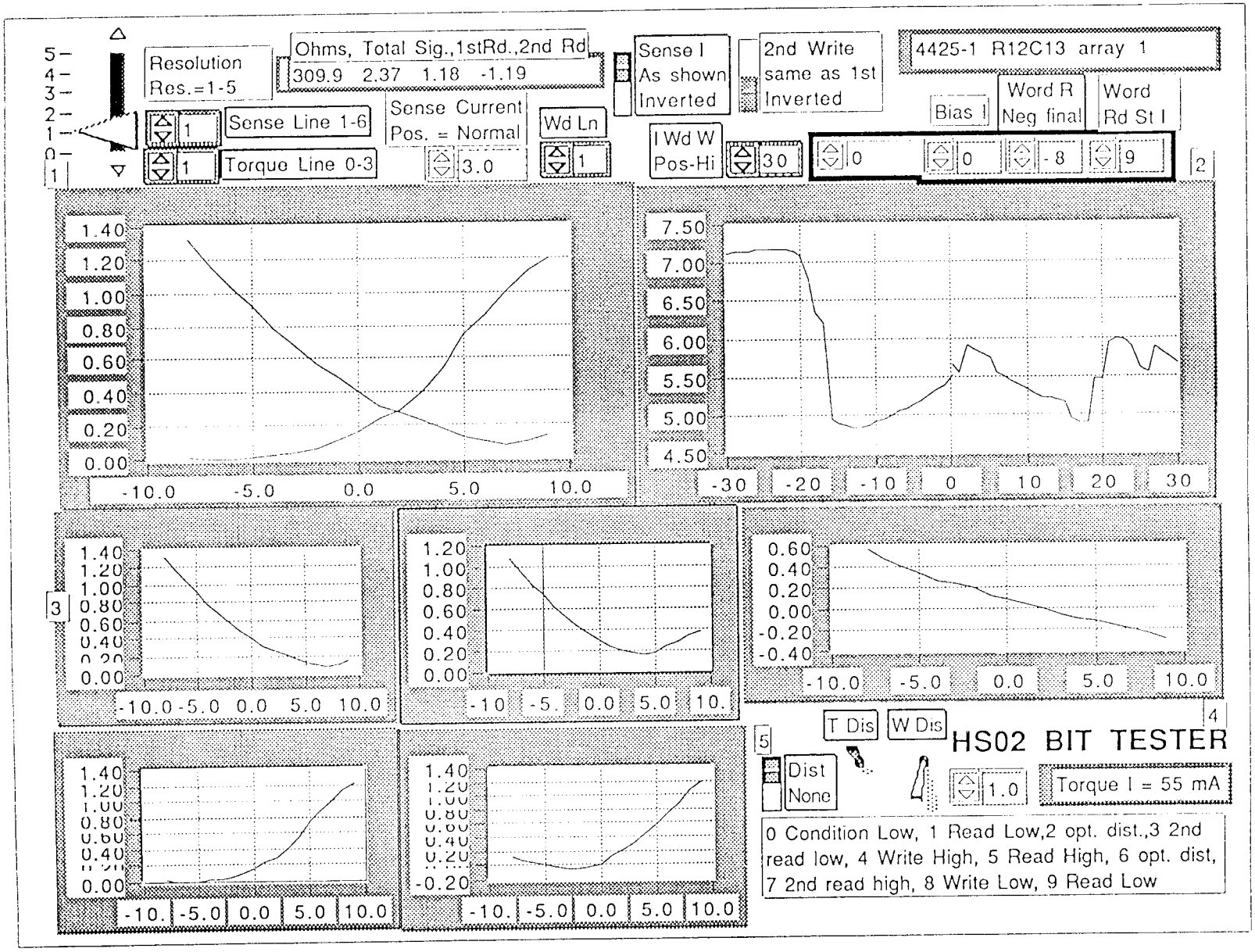


Fig 4

Front Panel

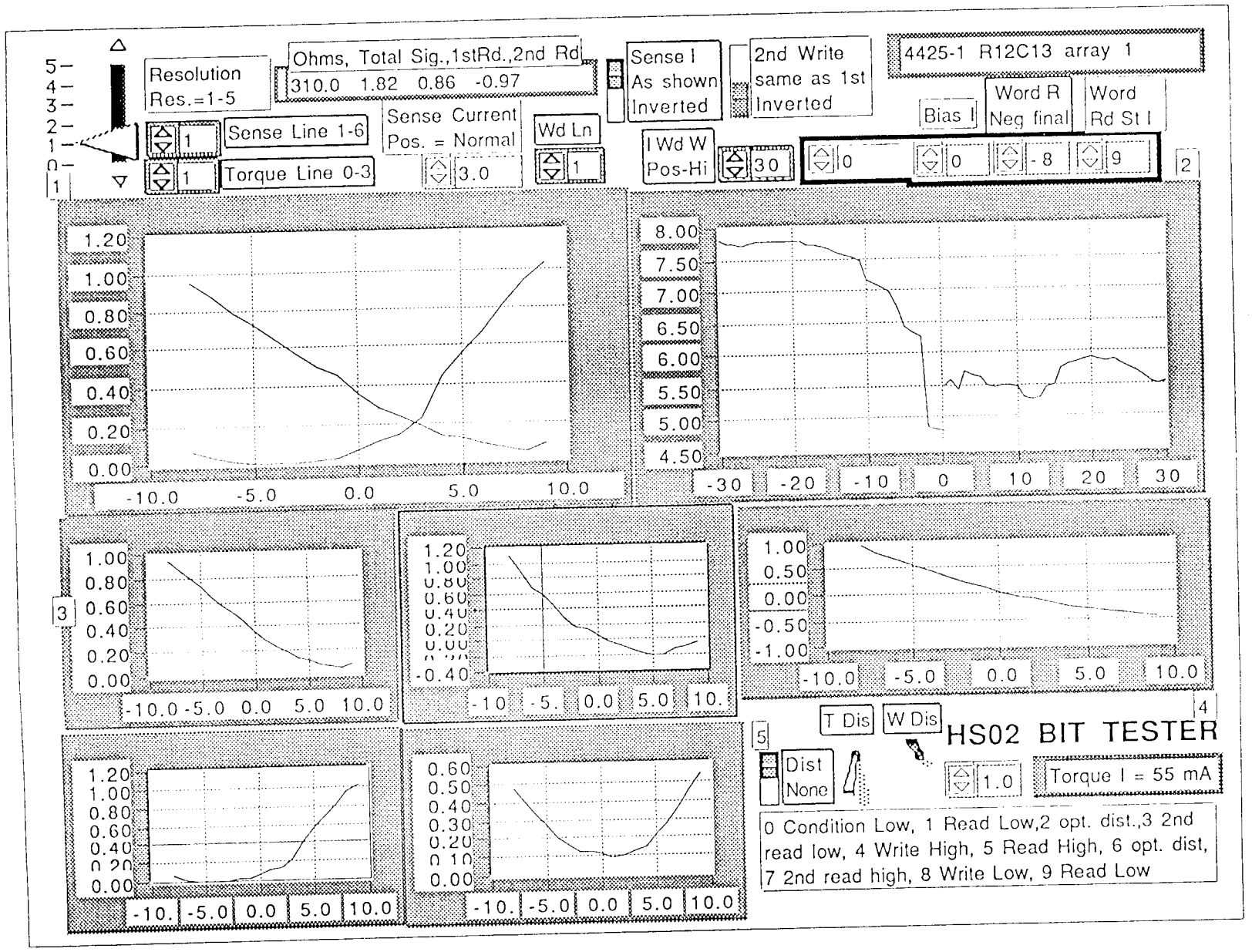


Fig. 5

Front Panel

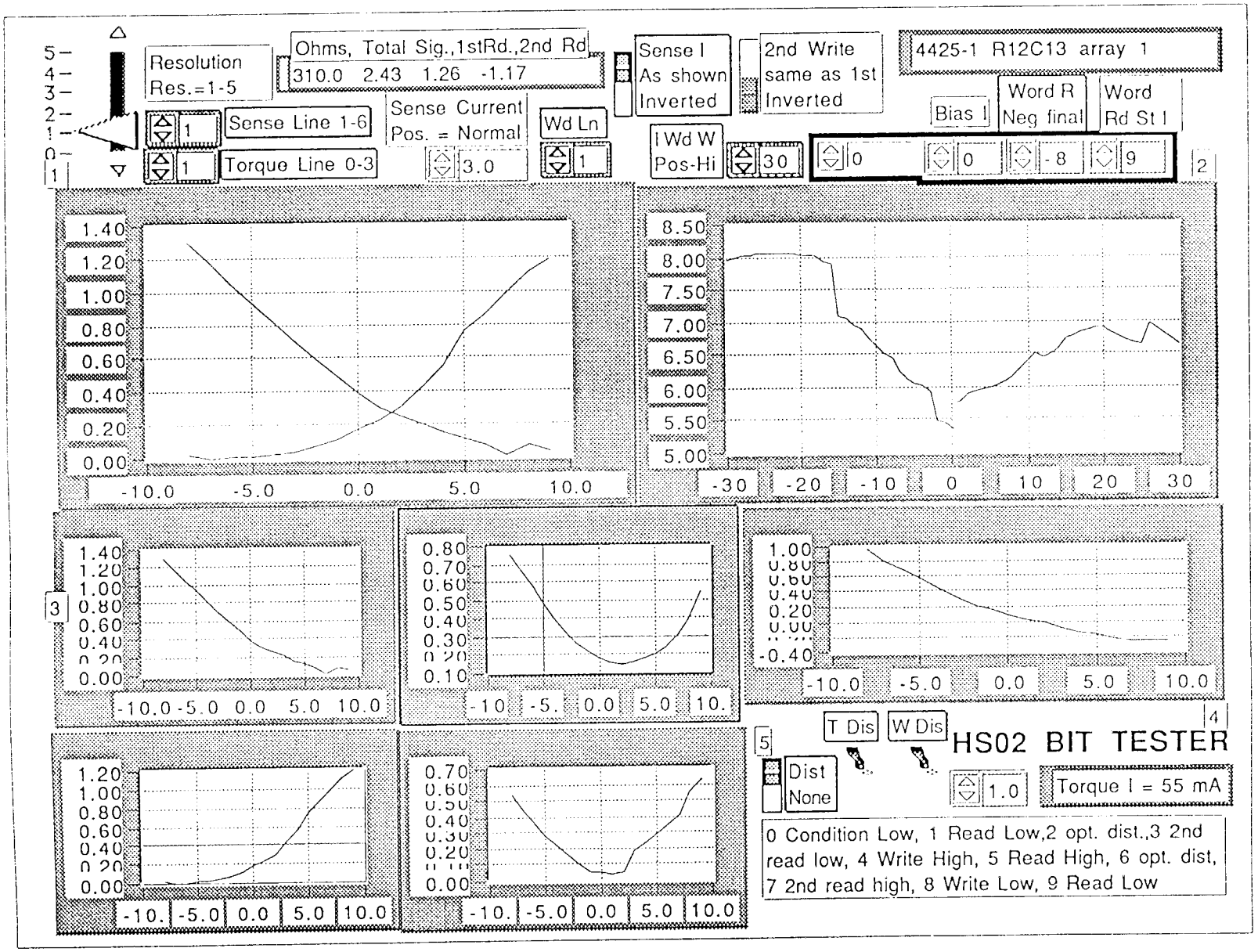


Fig. 6

NVE has drawn the following conclusions as a result of the Phase I work on the MRAM memory cells for an RFID applications:

1. The memory cells designed for use in this program satisfy the requirements for use in an RFID tag application.
2. Additional memory cell development will likely result in a lower power, higher signal design. This additional development will be bid into the Phase II proposal.

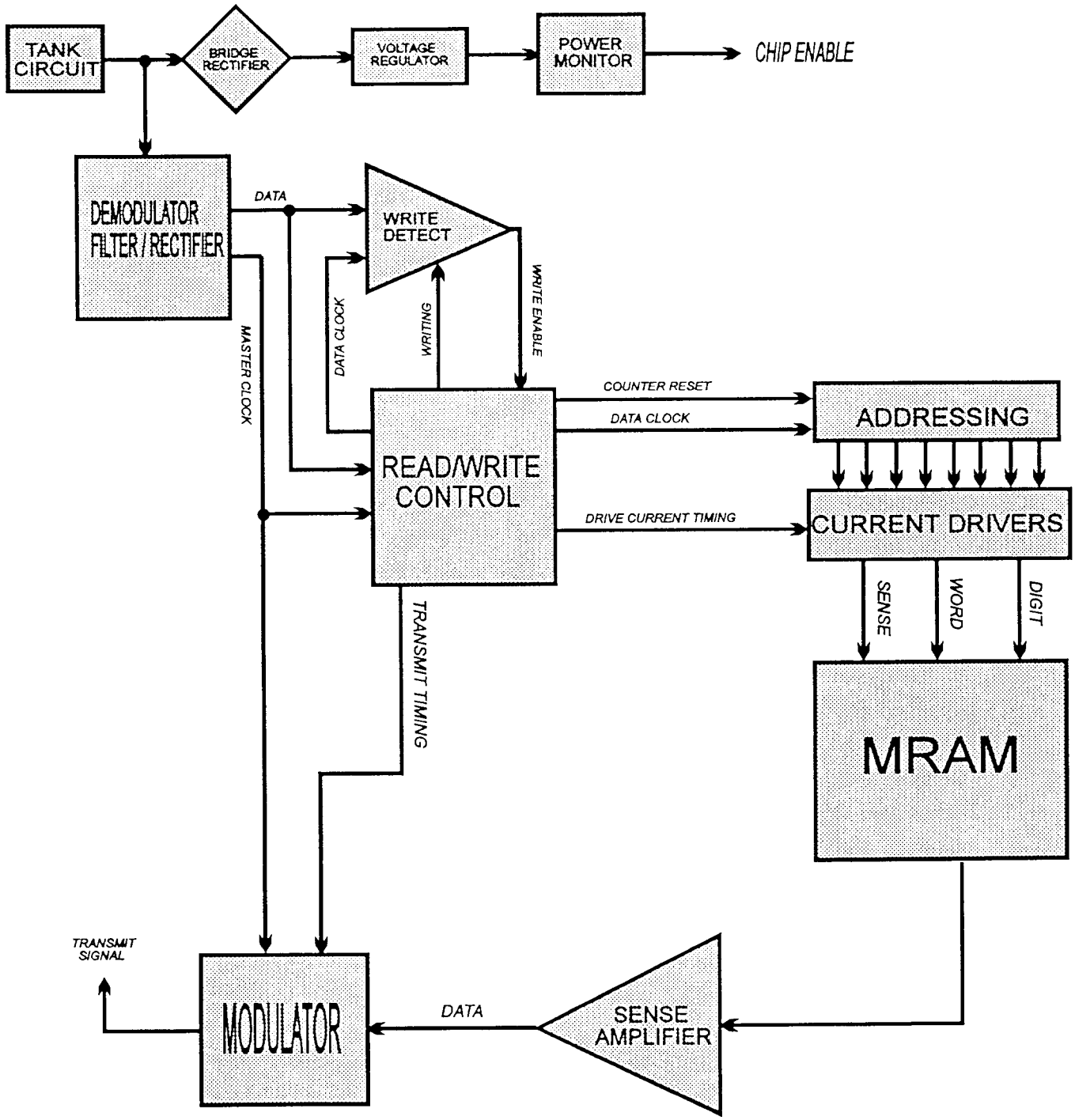
RFID Chip Circuitry - The circuitry designed during this portion of the program would be used on the RFID chip itself to receive the power from the transmitter, and convert it to usable voltage on the chip. It would also decode the read or write signal encoded on the transmission, and the data from the transmission if a write operation was detected. For a read operation, the chip would transmit back to the operator the data stored in the MRAM memory cells. For a write operation, the chip would store the data in a temporary buffer, then write this information to the MRAM memory cells, and transmit an 'OK' signal back to the operator indicating that the operation had been successfully completed.

Writeable RFID chips are currently sold as products, so the question addressed by this portion of the work is not if a writeable chip can be built, but whether CMOS or BiCMOS circuitry can be used to integrate an MRAM memory cell into a writeable RFID chip. The answer is clearly yes; the circuit design and simulation portion of this program went remarkably well, and NVE went beyond the original scope of the work(power supply interface circuitry and MRAM operational circuitry), and nearly completed the entire chip's circuit design.

The process used to define the transistor characteristics for this design is available from American Microsystems, Inc., in Pocatello Idaho. It is a BiCMOS process, so in addition to N-channel and P-channel MOS devices, there is a high quality NPN bipolar transistor available as well. The NPNs are important for the bridge rectifier and voltage regulator circuitry, and would provide additional gain in the sense amplifier if they were employed there; however, they are not absolutely required, and the chip could be built with a straight CMOS process if BiCMOS was not available.

Description of Chip Operation - This description will refer to the block diagram of the chip shown on the following page. Operation begins when a time-varying magnetic field of sufficient field strength begins transmitting in the proximity of the chip. The field is received through the on-chip antenna, which uses its own internal resistance and a bond-on chip capacitor to form an RLC resonant circuit, or a tank circuit as it is labelled in the block diagram. The output of the circuit across the capacitor is connected to the bridge rectifier circuit and a 370 pF on-chip capacitor to generate the on-chip power supply. Four diode connected NPN transistors are used to form the diode bridge required for the bridge rectifier circuit. The electrical output of the bridge rectifier circuit can be seen in the first section of this report; all the antenna simulations done early in this Phase I work assumed this bridge rectifier on the output of the tank circuit.

RFID ARCHITECTURE BLOCK DIAGRAM



The on-chip voltage regulator circuit is comprised of a bandgap voltage reference and an amplifier for regulator control. Depending upon the match of the resistors in the amplifier inputs, the on-chip voltage can be regulated anywhere from 2 to 5.5 volts. The remainder of the circuitry on the chip was designed using a 5V +/- 10% supply. The voltage regulator's output is monitored by the power monitor circuitry. This circuit ensures that if the voltage falls below a minimum safe level, in this case 3.5 volts, any read or write cycles are interrupted and an error message is transmitted to the operator.

The output of the tank circuit is also directed to the demodulator circuitry. This circuitry decodes the control and data signal superimposed on the input signal, and also uses the input signal frequency to generate a master system clock. This clock is used to generate the rest of the signals required for reading and writing the MRAM memory array. The demodulator and modulator circuitry are among the most critical in this design, and a separate report covering this circuit is included at the end of this section.

The demodulated control signals are piped to the write detect circuitry; this block provides a signal to the read/write control circuits that specifies whether a read or a write operation is beginning. Timing signals are generated by the read/write control that addresses the MRAM memory array, and turn on the current drivers required for the MRAM read/write operations. For a read cycle, the data is read out of the MRAM array in serial fashion. During a write cycle, the incoming data is stored in a shift register and written into the MRAM memory array one bit at a time.

During a read operation, a counter increments the addressing circuitry and one MRAM memory cell is read on each cycle. The signal from the memory cell is fed to the sense amplifier circuitry, where it is converted to a digital signal. This signal is used by the modulator circuitry to modulate the voltage on one node of the tank circuit, and therefore broadcast a signal back to the operator on a lower frequency than the transmit frequency. Typical charge times for the power supply after a read or write operation are 10-25 microseconds, meaning that for 128 bits the entire cycle is complete in just over 3 milliseconds.

A more detailed look at the modulator/demodulator(which is not complete) is given on the eight pages following the end of this section. The circuit schematics are shown as an appendix to this section. HSPICE simulations have been performed on all circuits in the appendix to verify proper operation, but they have not been included because they could easily swell the page count of this report by more than 100.

The conclusions reached as a result of this Phase I work regarding the circuit design of this writeable RFID chip are as follows:

1. The circuitry required to interface the on-chip antenna to a power supply for the RFID chip can be accomplished without serious difficulty.
2. The power supply generated for the chip is capable of supplying the energy required for MRAM read/write operations.
3. The remainder of the circuitry required for a complete RFID chip is straightforward circuit engineering, and will not be an obstruction to completing a working prototype part.

Preliminary Transponder Modulator & Demodulator Design

Introduction

Existing nonwritable transponder tags generally use a unidirectional phase modulated encoding scheme to transmit data from the tag to the outside world. The tag is energized by a fairly high intensity fixed frequency local rf field which provides both power and clock information to the tag. Once power is detected in the tag, data is shifted out to the transmit/receive coil, which transmits back at a subharmonic of the original stimulus rf frequency. By choosing the tag transmit frequency to be half of the stimulus frequency, the same coil may be used for both transmitting and one of the difference product falls back in-band, resulting in at least some increase in apparent useful transmit power. For the writable tag application, there is no reason to alter this well established scheme - except perhaps in the frequency of operation. The real issue here is how to best address the transponder data receiver, which must operate continuously from only received rf power and which must consume very little of the available power budget.

Review of Typical Tag Phase Shift Modulation Scheme

A fairly clear explanation of a popular Tag read-out scheme is presented in the Troyk et al. patent (5,198,807). A block diagram of the transponder is presented in Fig. X1, the external receiver is shown in Fig. X2, and the associated waveforms during typical operation are shown in Fig. X3. The signal across the loop antennae (labeled A in Fig. X3) is detected by the clock recovery circuit which produces a near square wave at the stimulus frequency. When transponder transmitting is enabled, one side of the coil is grounded during 1/2 of either even or odd clock cycles depending upon the data to be transmitted (see waveform C). This phase modulates the return signal relative to the stimulus signal and results in the external receiver waveforms G-K.

Proposed Tag Receiver Scheme

For the writable tag, data rates to and from the tag need only be a few hundred Baud and only half duplex communication is really needed. Of the many possible modulation schemes, a frequency shift method (FSK) appears to provide the best combination of allowing continuous input power to the tag and reasonable receiver complexity and required power. In comparison with other circuit components of the tag, the receiver power dissipation is uniquely important in that it must usually be powered-up when the rf field is applied.

This proposed circuit is a fairly conventional PLL FSK demodulator method with a switched-capacitor loop filter and output comparator. For operation with a stimulus frequency range of 1.7 - 1.9 Mhz, a free-running oscillator frequency of nominally 1.8Mhz would be used with possibly a 50 KHz difference between mark and space frequencies. A block diagram of the proposed demodulator is shown in Fig. X4.

Provided that at least a few tens of microamps of power are available and the data bandwidth is limited to a few hundred Baud, there appear to be few fundamental technical risks with this scheme. As a design exercise, a VCO was designed for the nominal near 2 Mhz center frequency in a conventional 2 micron CMOS process. In order to minimize required power and fully utilize anticipated chip resources, a self-retriggered one-shot circuit is proposed. An on-chip capacitor is simply charged up via a PTAT current source and reset upon it passing approximately the bandgap voltage. This scheme appears to be more process stable than a simple relaxation oscillator and requires less power than a stabilized ring-oscillator (Young cite). A schematic of this circuit is presented in Figs. X5 and X6. Based upon SPICE simulations, this circuit will only consume 30-50 uW when active and can easily accommodate the required oscillation range of about 2MHz.

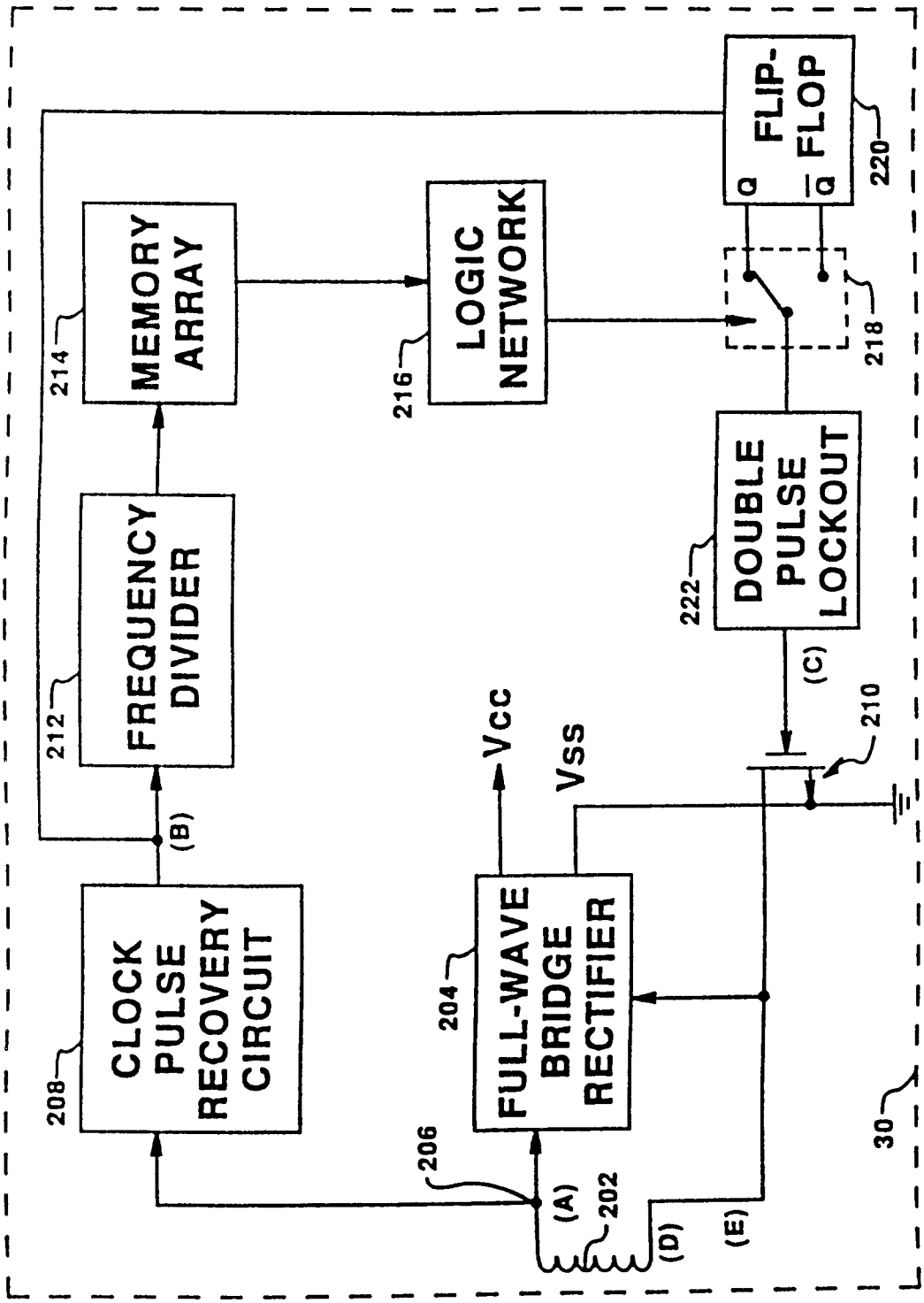
The specifics of the filter circuit remain to be determined, but it appears that a lag-lead filter (matched numbers of pole(s) and zero(s)) would probably provide the most optimal detector performance (wide tracking range and narrow detector bandwidth). (See for example, Grebene, pp. 634-668). The details of the phase detector also need to be determined, although the use of a simple XOR type circuit is anticipated. For the comparator, a switched capacitor windowed comparator which autozeros against the VCO control voltage once or more per bit period, and which then compares against subsequent control voltages would probably be used. (Providing outputs upon shifts in input frequency.)

Cites

Will probably include a few patent cites here

[1] Ian Young, et.al., "A PLL clock generator with 5 to 110 Mhz of lock range for microprocessors", IEEE Journal of Solid-State Circuits, vol. 27, no. 11, November 1994, pp. 1599-1607.

[2] Alan Grebene, Bipolar and MOS analog integrated circuit design, Wiley, NY 1983.


FLIP-FLOP
Q
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MEMORY ARRAY
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LOGIC NETWORK
216
218
DOUBLE PULSE LOCKOUT
222
FREQUENCY DIVIDER
212
(C)
210
V_{CC}
V_{SS}
(B)
CLOCK PULSE RECOVERY CIRCUIT
208
FULL-WAVE BRIDGE RECTIFIER
204
206
(A)
202
(D)
(E)
30

Fig. 5

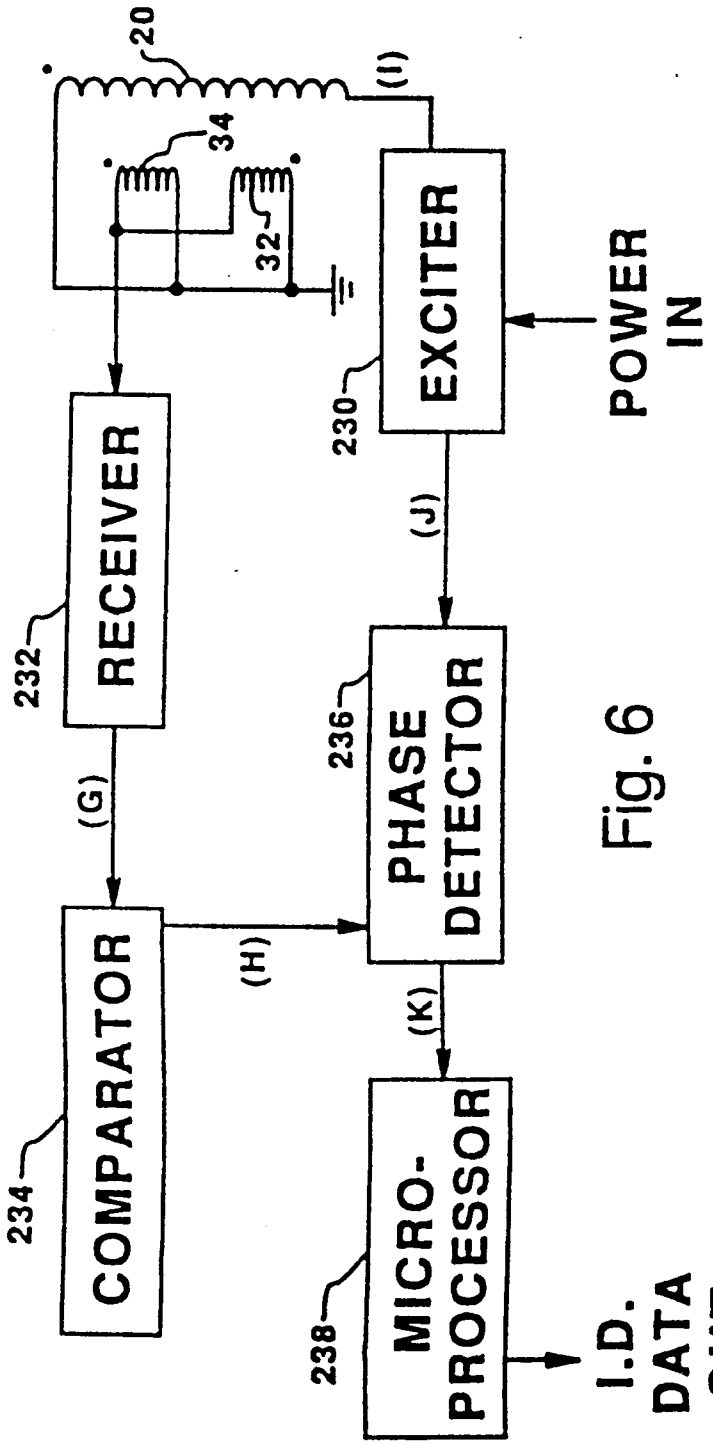

20
(I)
34
32
EXCITER
230
POWER IN
RECEIVER
232
(J)
(G)
PHASE DETECTOR
236
COMPARATOR
234
(H)
(K)
MICRO-PROCESSOR
238
I.D. DATA OUT

Fig. 6

F, 5, K2

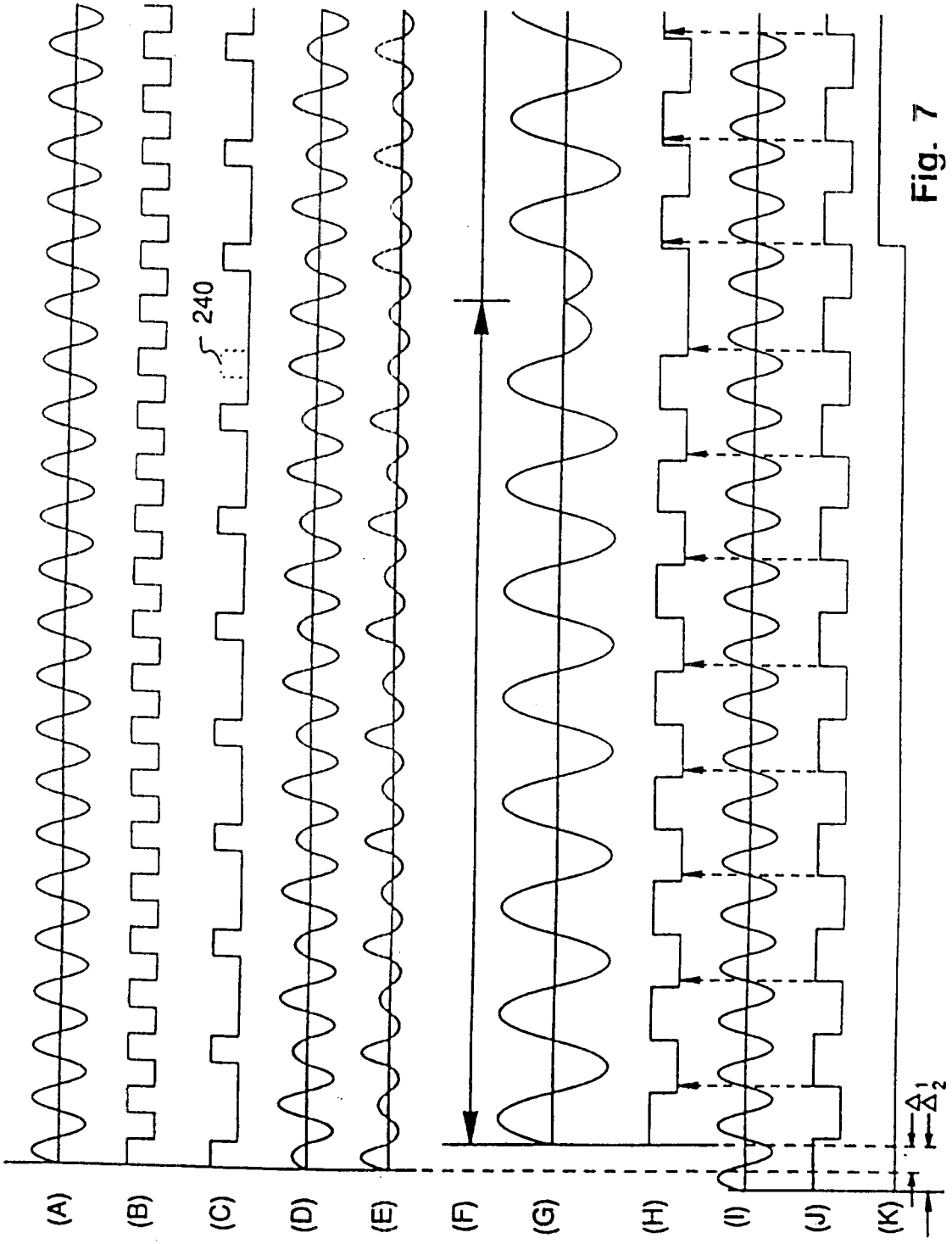


Fig. 7

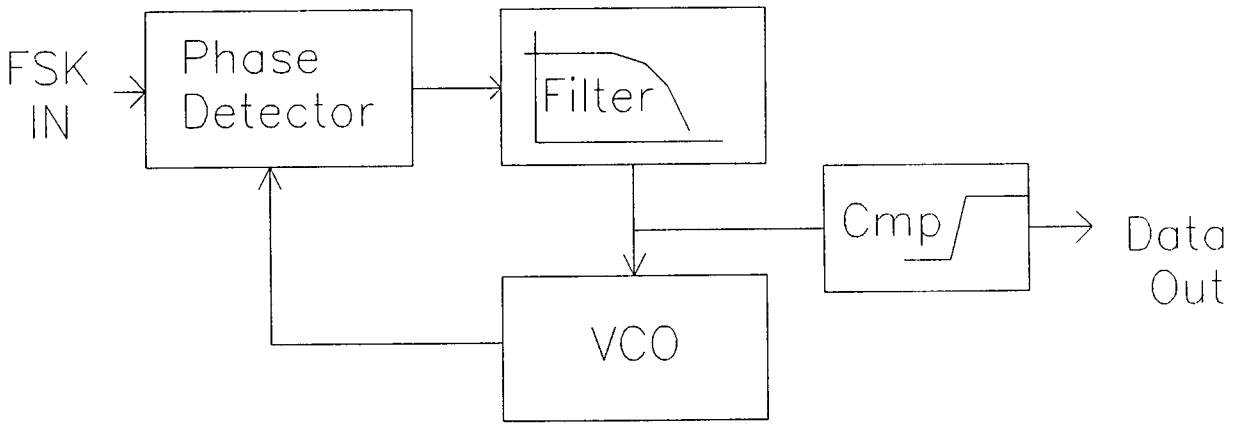
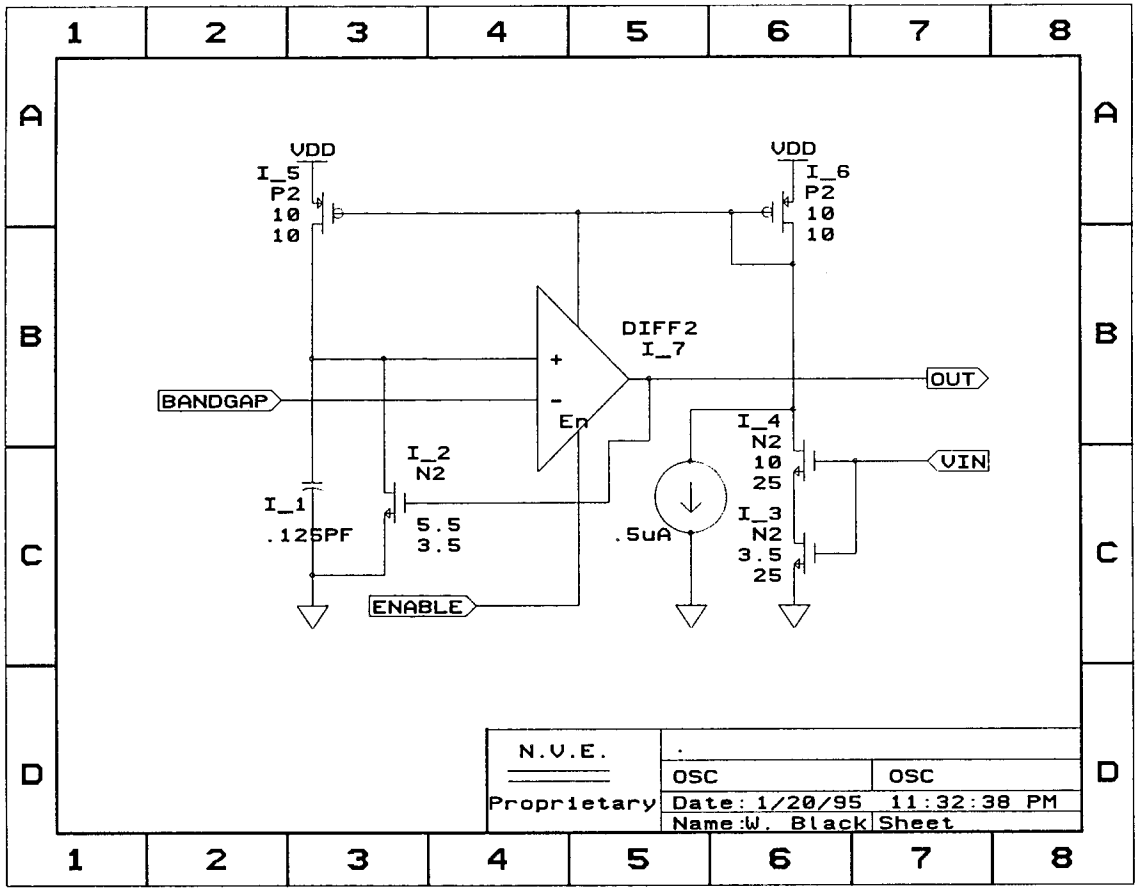


Fig. X4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3
4
5
6
7
8
A
B
C
D
VDD
I_5
P2
10
10
VDD
I_6
P2
10
10
DIFF2
I_7
+
-
En
BANDGAP
OUT
VIN
I_4
N2
10
25
I_3
N2
3.5
25
I_2
N2
5.5
3.5
I_1
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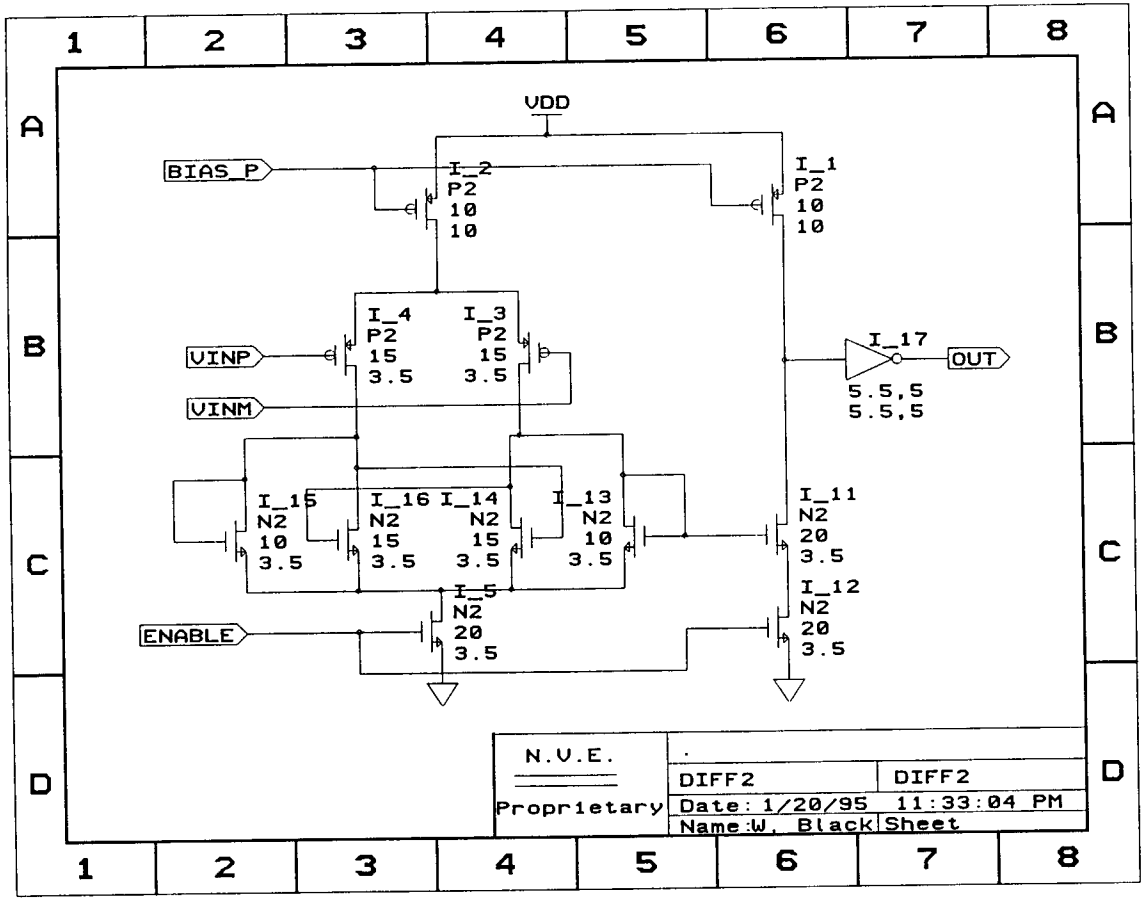
Fig. X.5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5
6
7
8
A
B
C
D
VDD
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P2
10
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P2
10
10
I_4
P2
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3.5
I_3
P2
15
3.5
VINP
VINM
I_17
OUT
5.5,5
5.5,5
I_15
N2
10
3.5
I_16
N2
15
3.5
I_14
N2
15
3.5
I_13
N2
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I_11
N2
20
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I_12
N2
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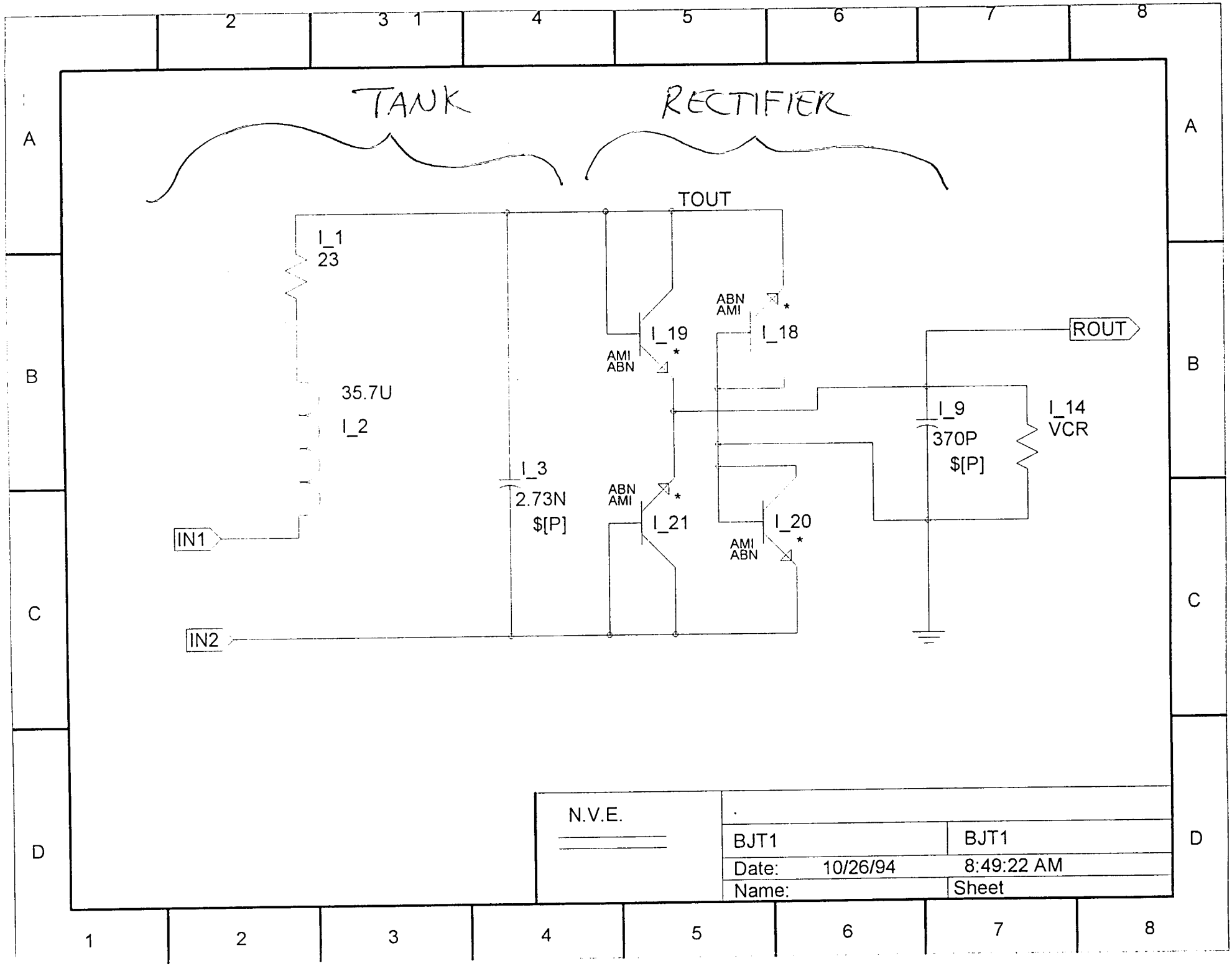
Fig. 16

Appendix to Circuitry Section of the Report

Circuit Schematics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IN2
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ABN
*
ABN
AMI
I_18
ABN
AMI
I_21
*
I_20
AMI
ABN
ROUT
I_9
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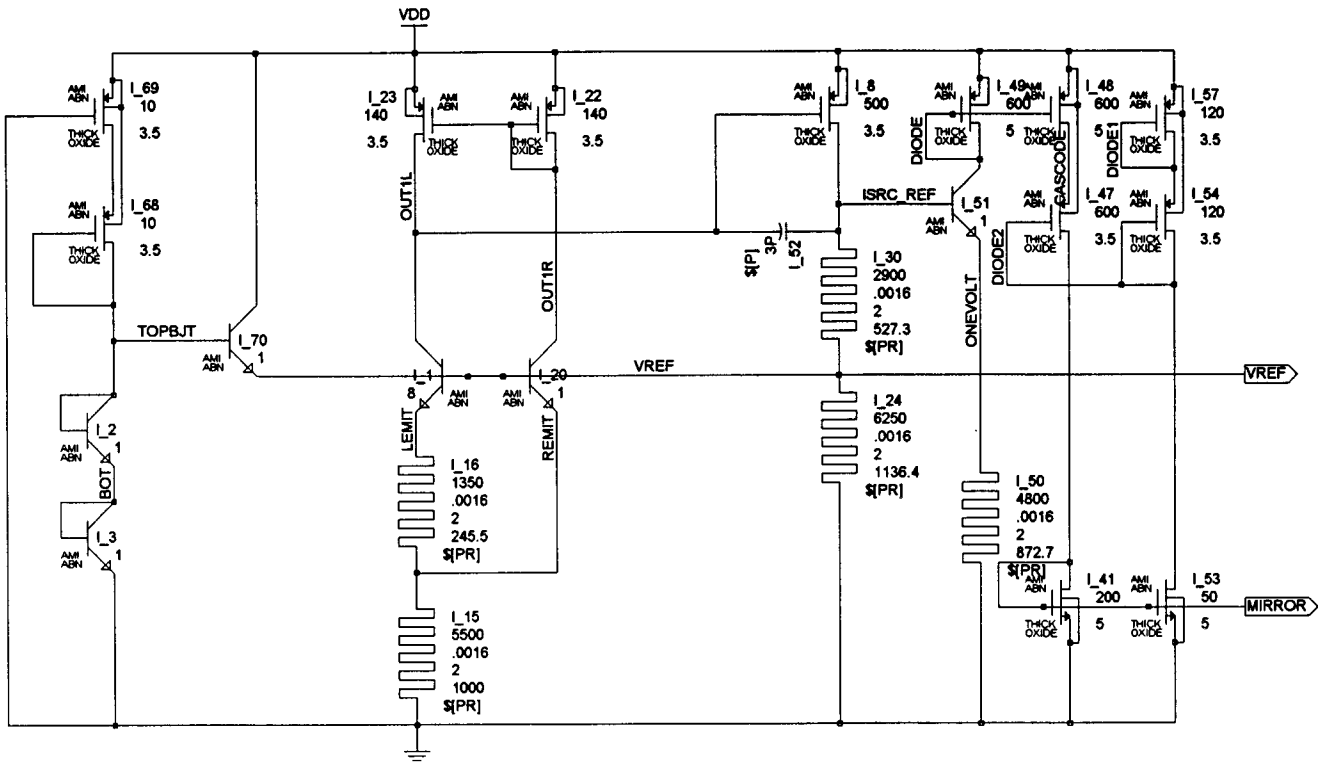

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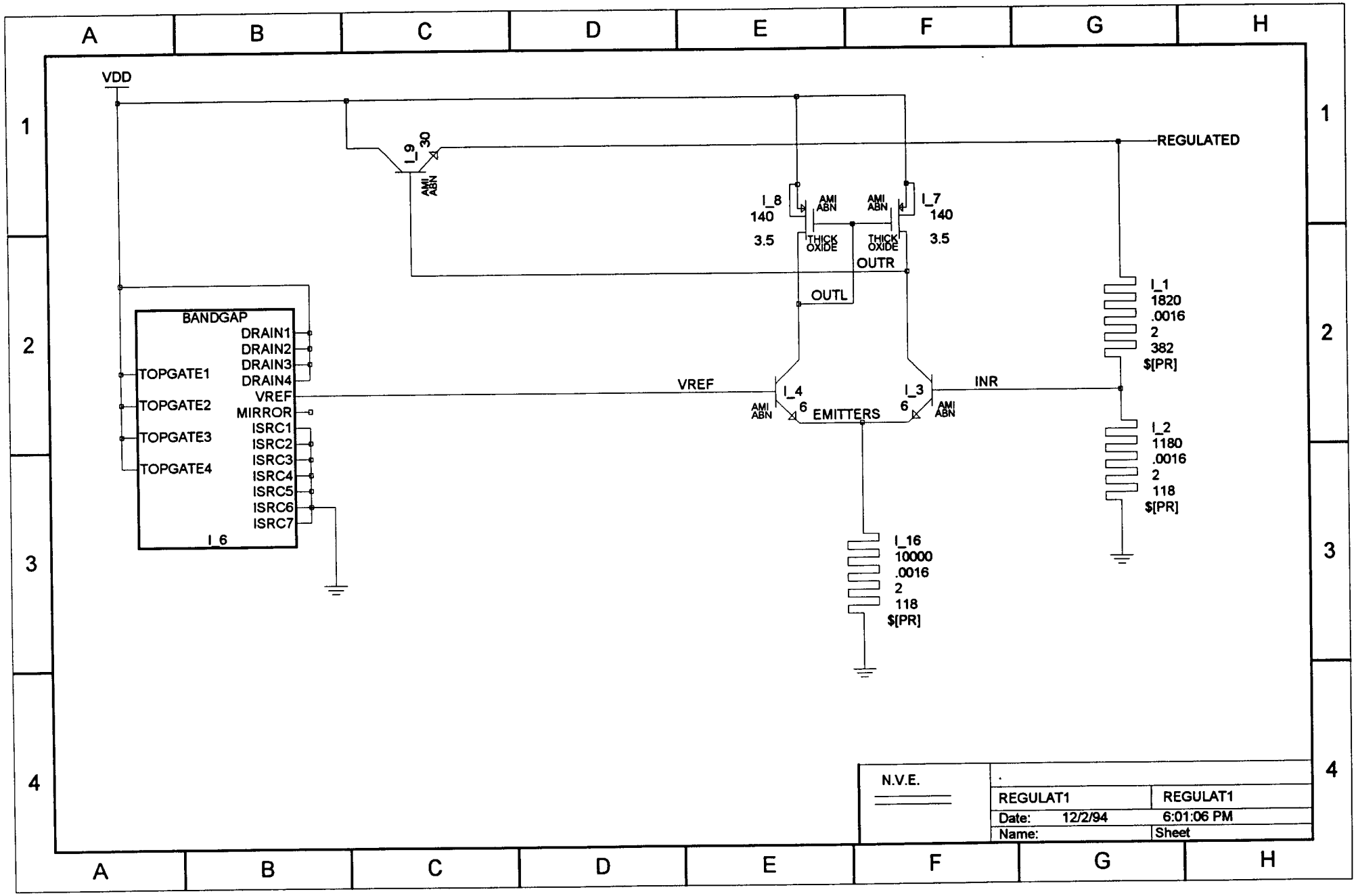
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I_8
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AMI ABN
THICK OXIDE
AMI ABN
THICK OXIDE
I_7
140
3.5
OUTR
OUTL
I_1
1820
.0016
2
382
$[PR]
BANDGAP
DRAIN1
DRAIN2
DRAIN3
DRAIN4
VREF
MIRROR
ISRC1
ISRC2
ISRC3
ISRC4
ISRC5
ISRC6
ISRC7
TOPGATE1
TOPGATE2
TOPGATE3
TOPGATE4
I_6
VREF
I_4
6
AMI ABN
EMITTERS
I_3
6
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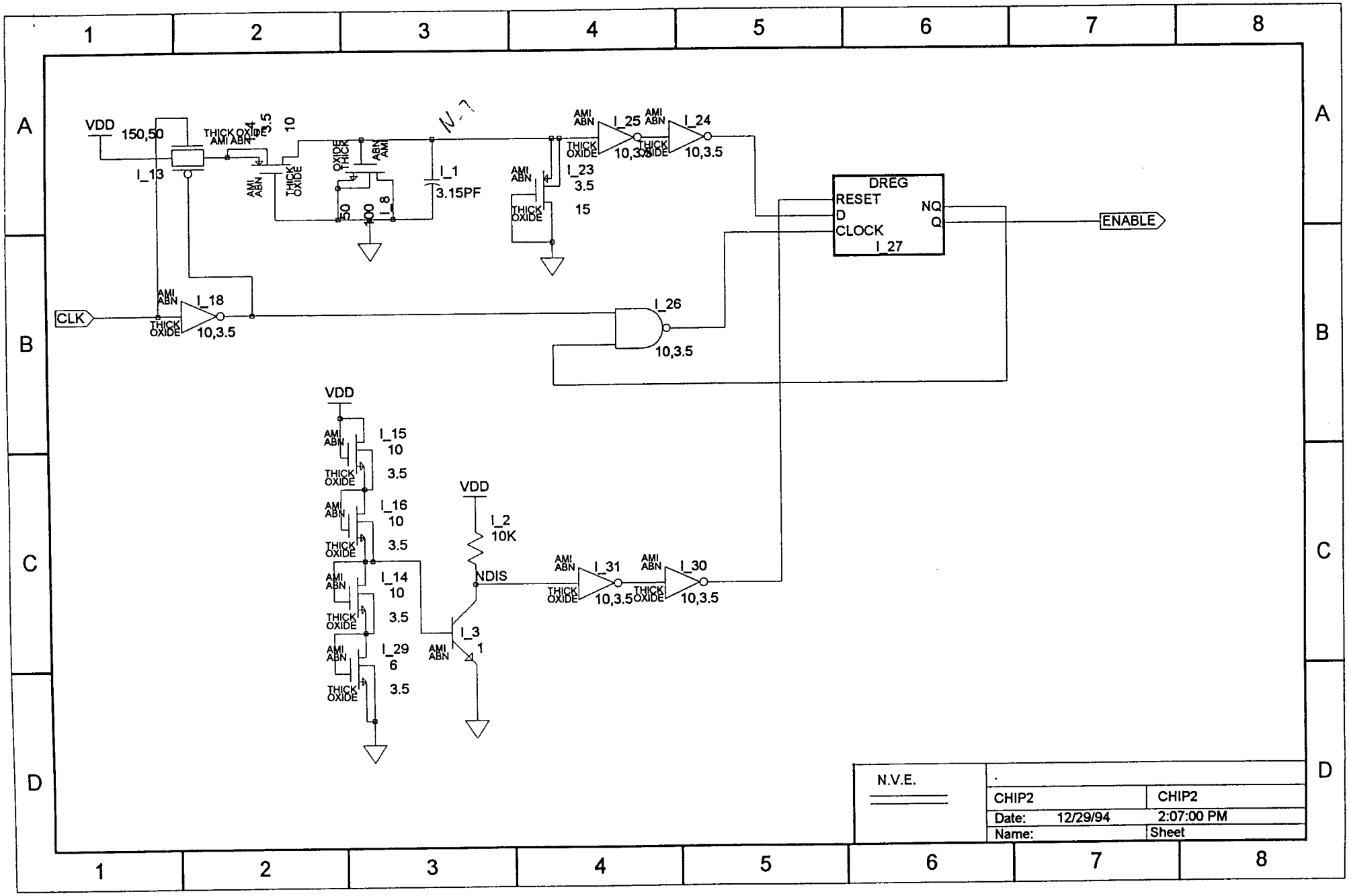
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B
C
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I_1
3.15PF
I_8
I_23
3.5
15
I_25
I_24
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D
CLOCK
I_27
NQ
Q
ENABLE
CLK
I_18
I_26
I_15
I_16
I_14
I_29
6
I_2
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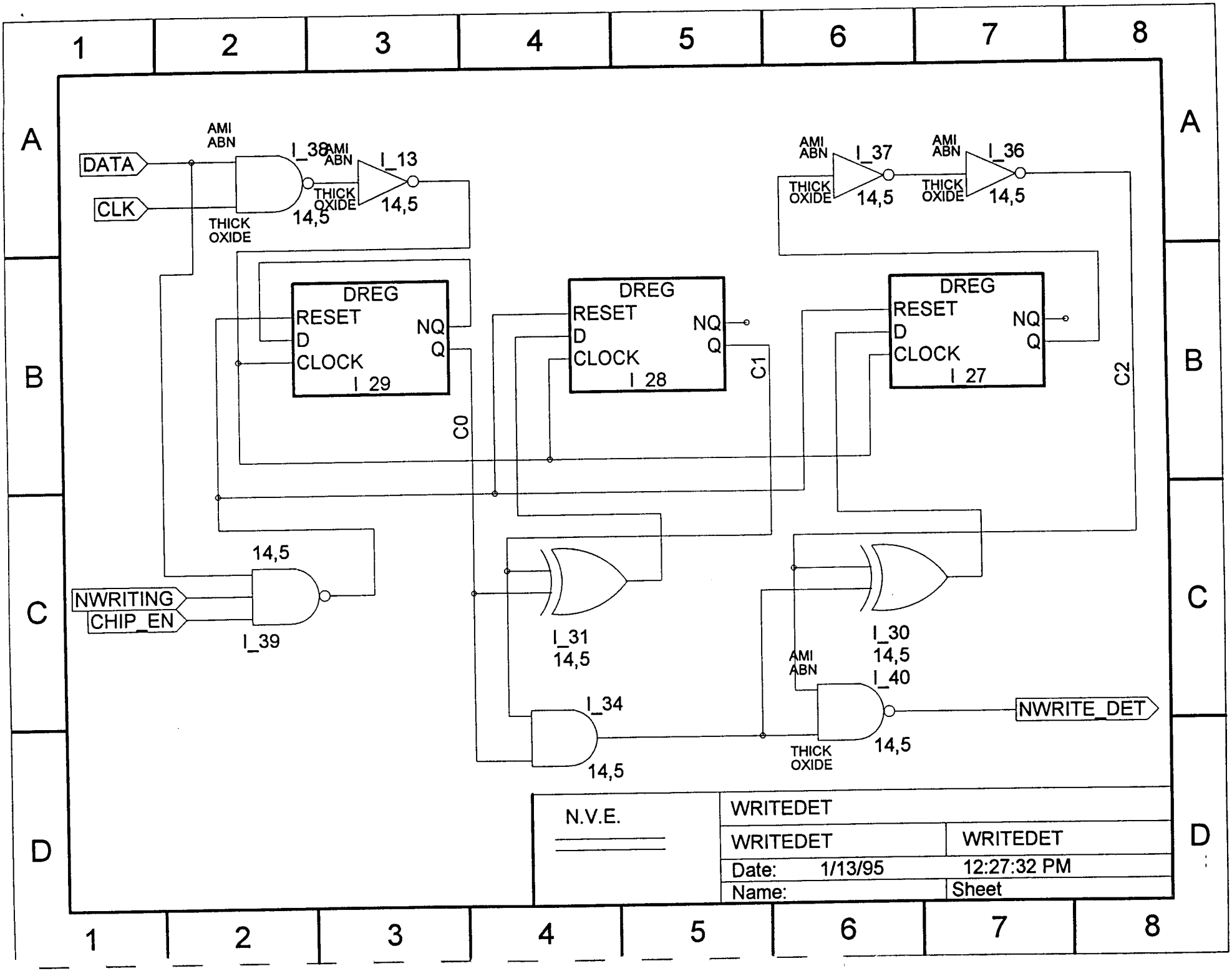
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C
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AMI
ABN
I_13
THICK
OXIDE
14,5
AMI
ABN
I_37
THICK
OXIDE
14,5
AMI
ABN
I_36
THICK
OXIDE
14,5
DREG
RESET
D
CLOCK
NQ
Q
I_29
DREG
RESET
D
CLOCK
NQ
Q
I_28
DREG
RESET
D
CLOCK
NQ
Q
I_27
C0
C1
C2
NWRITING
CHIP_EN
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I_39
I_31
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I_30
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I_40
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ABN
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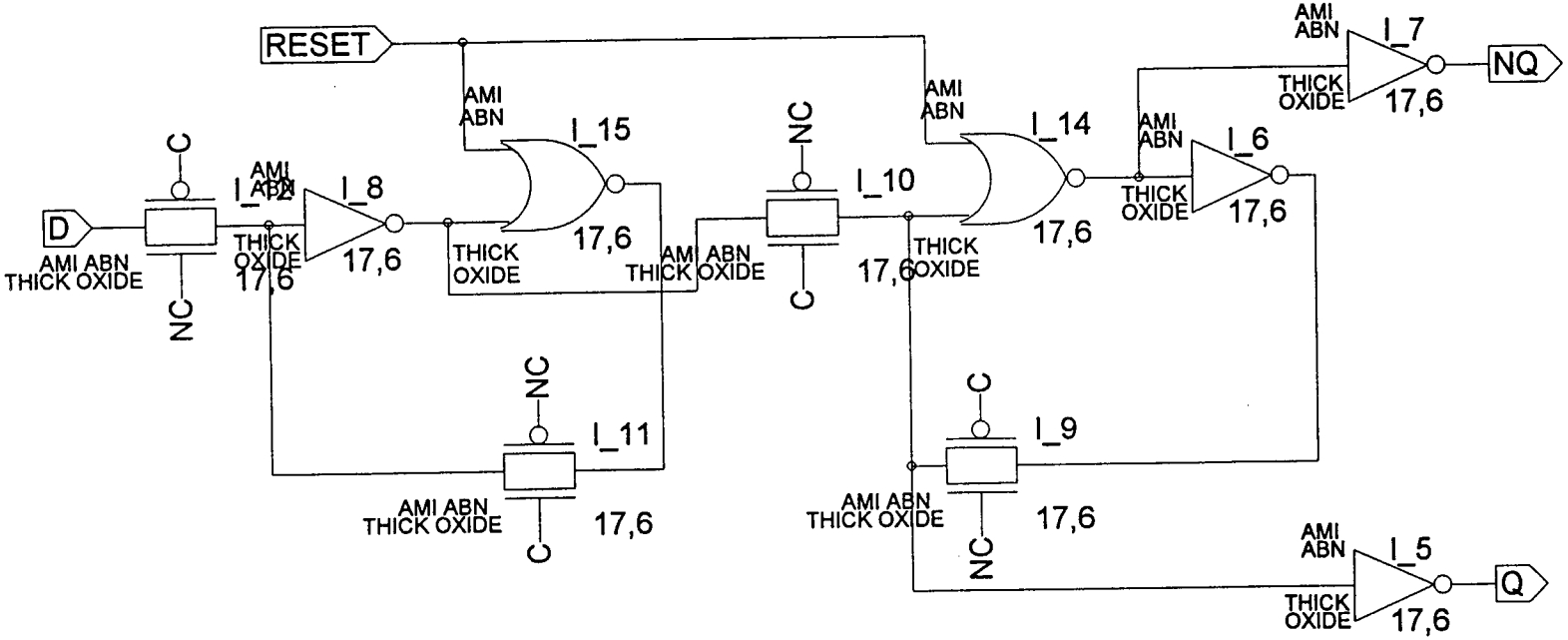

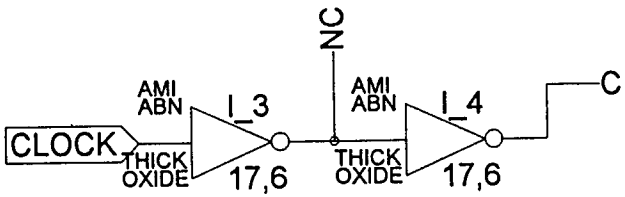

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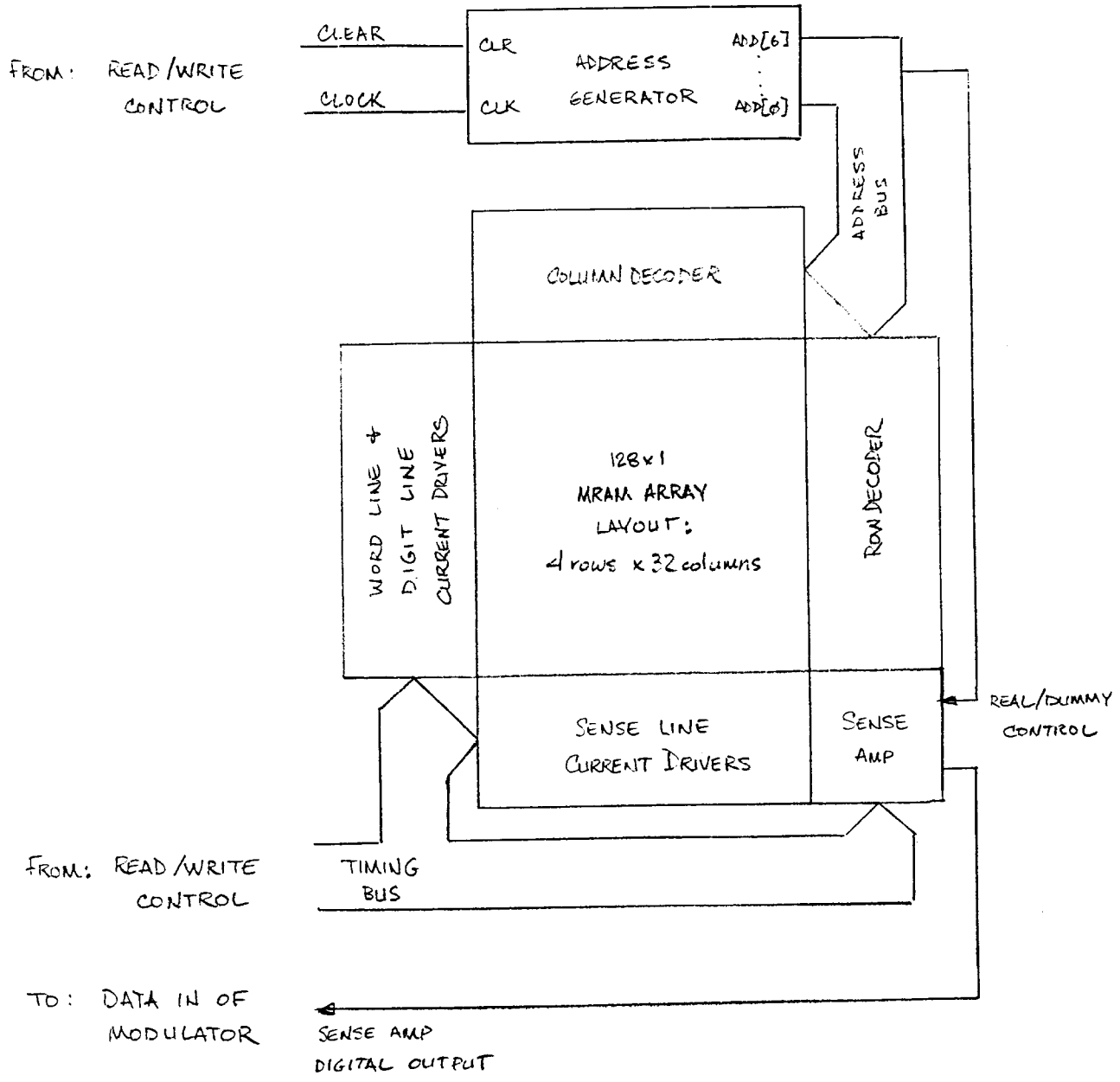

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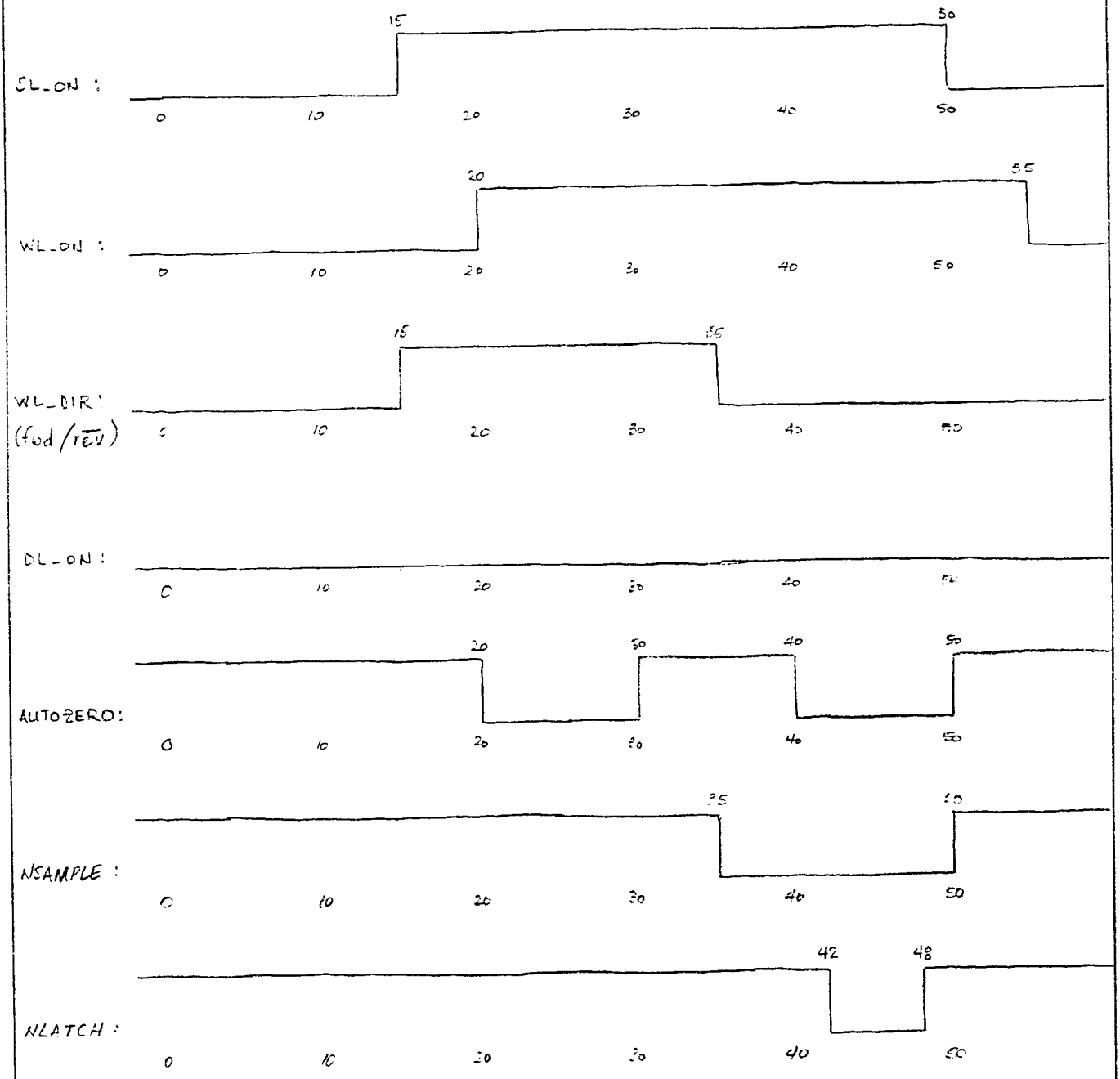

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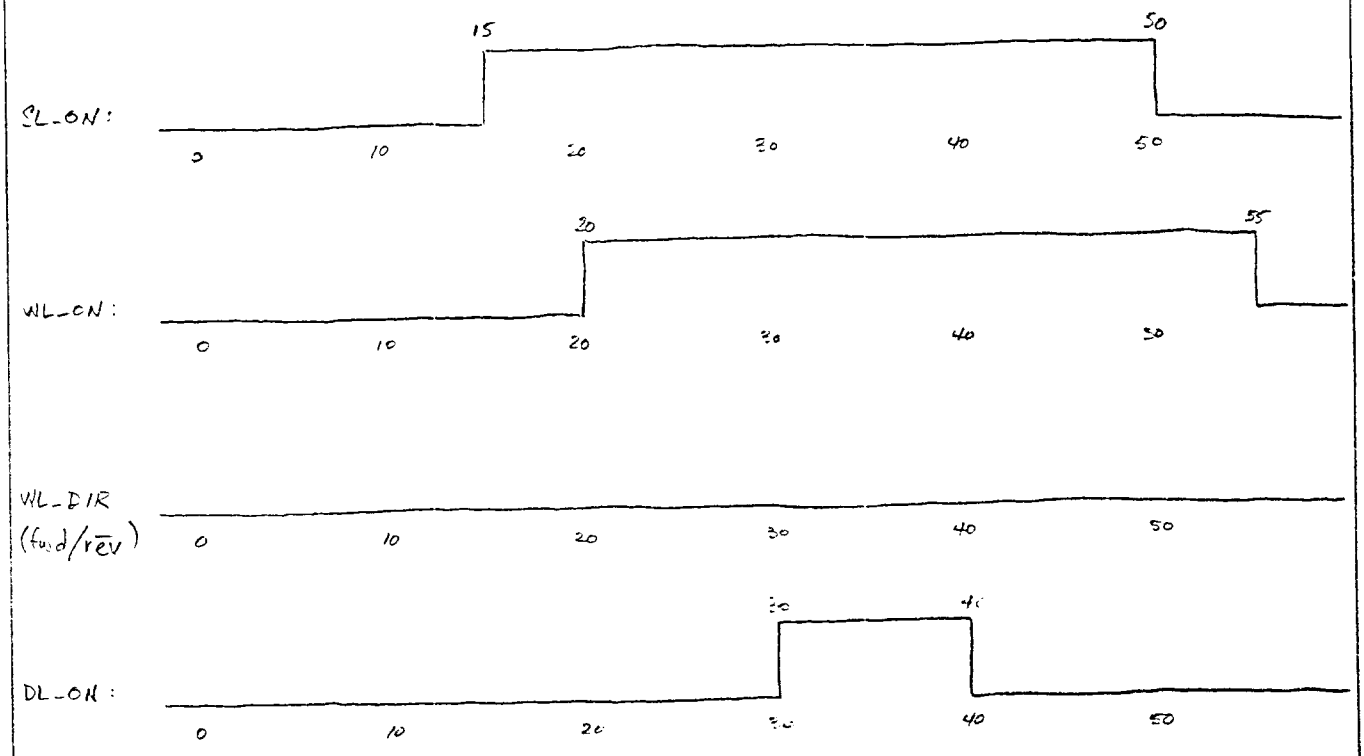

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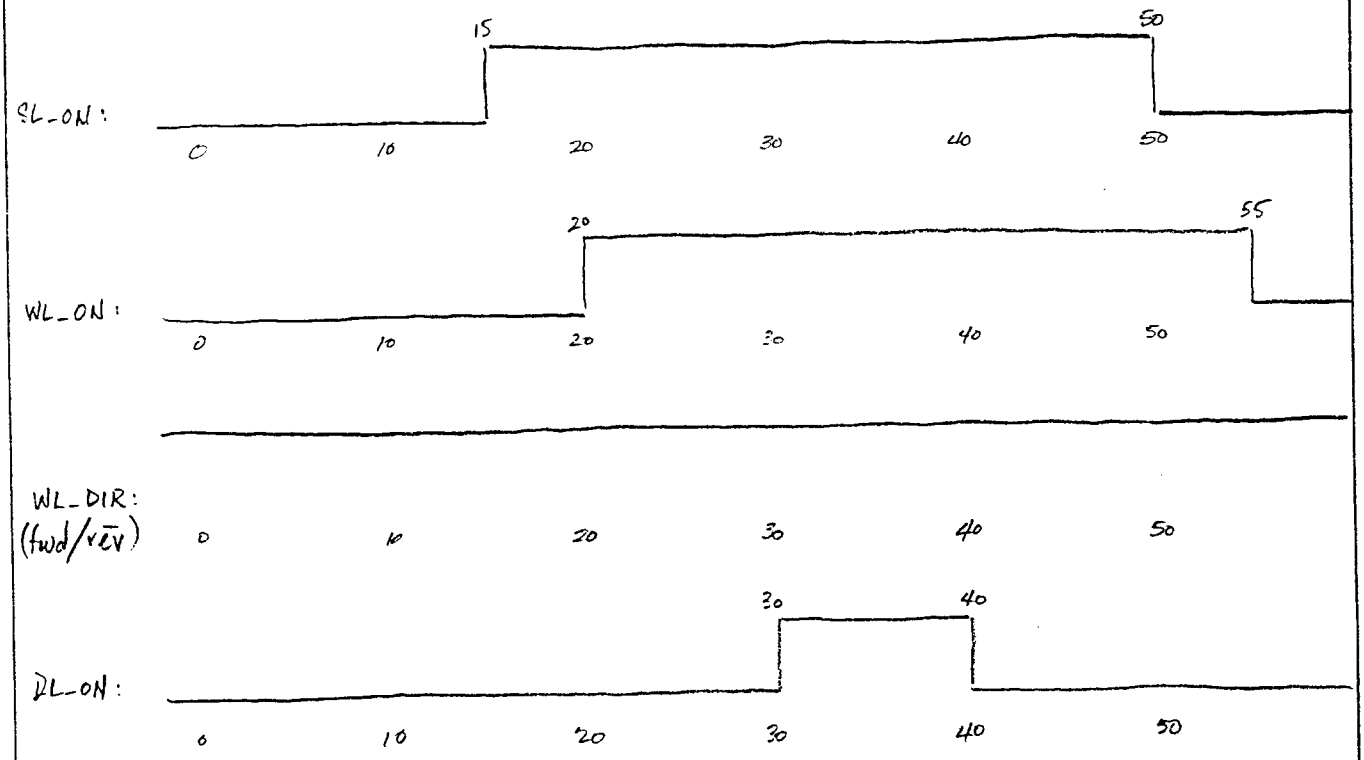

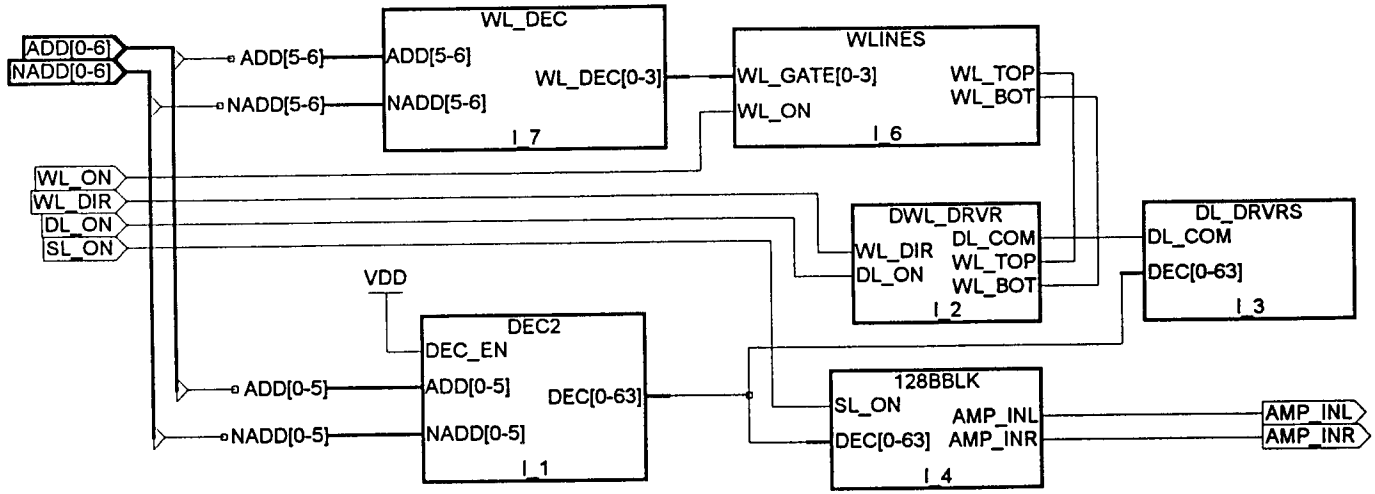

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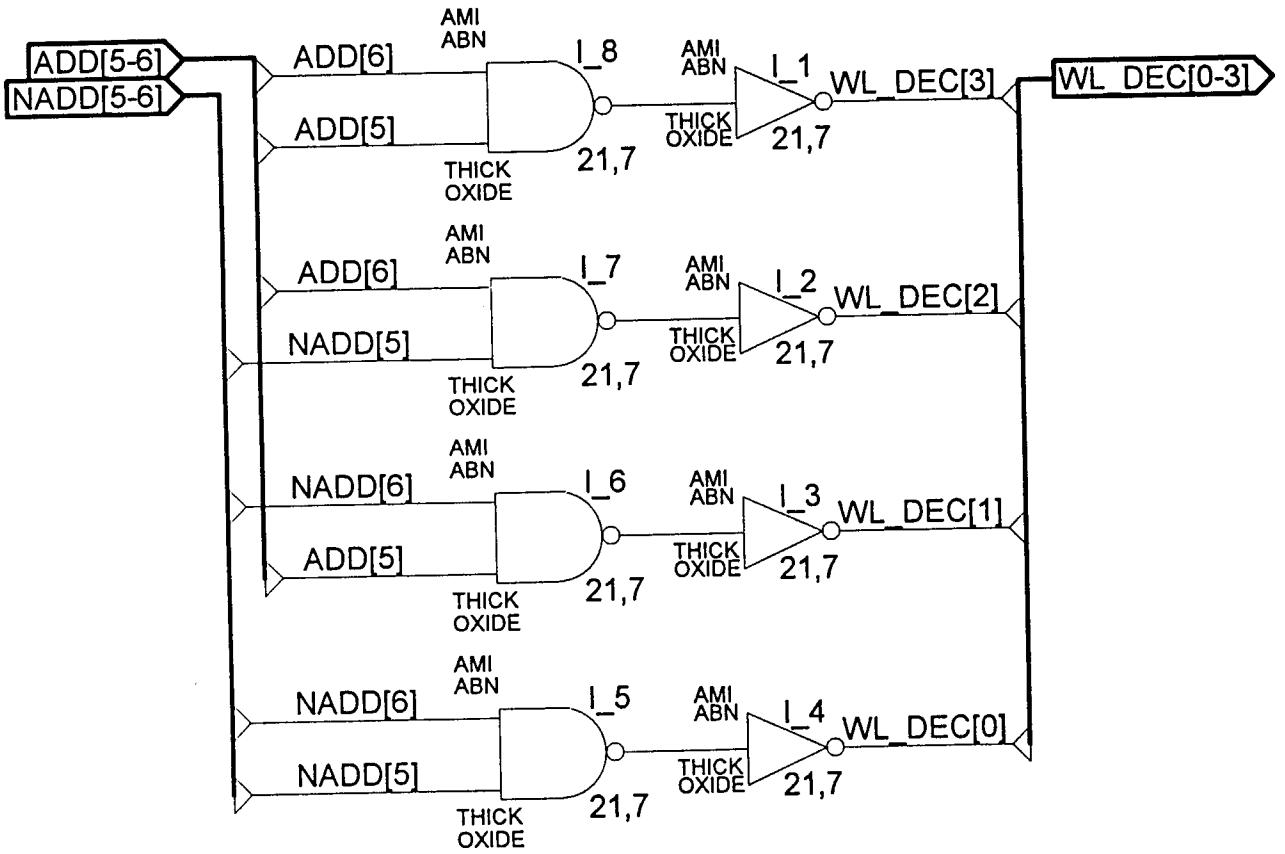

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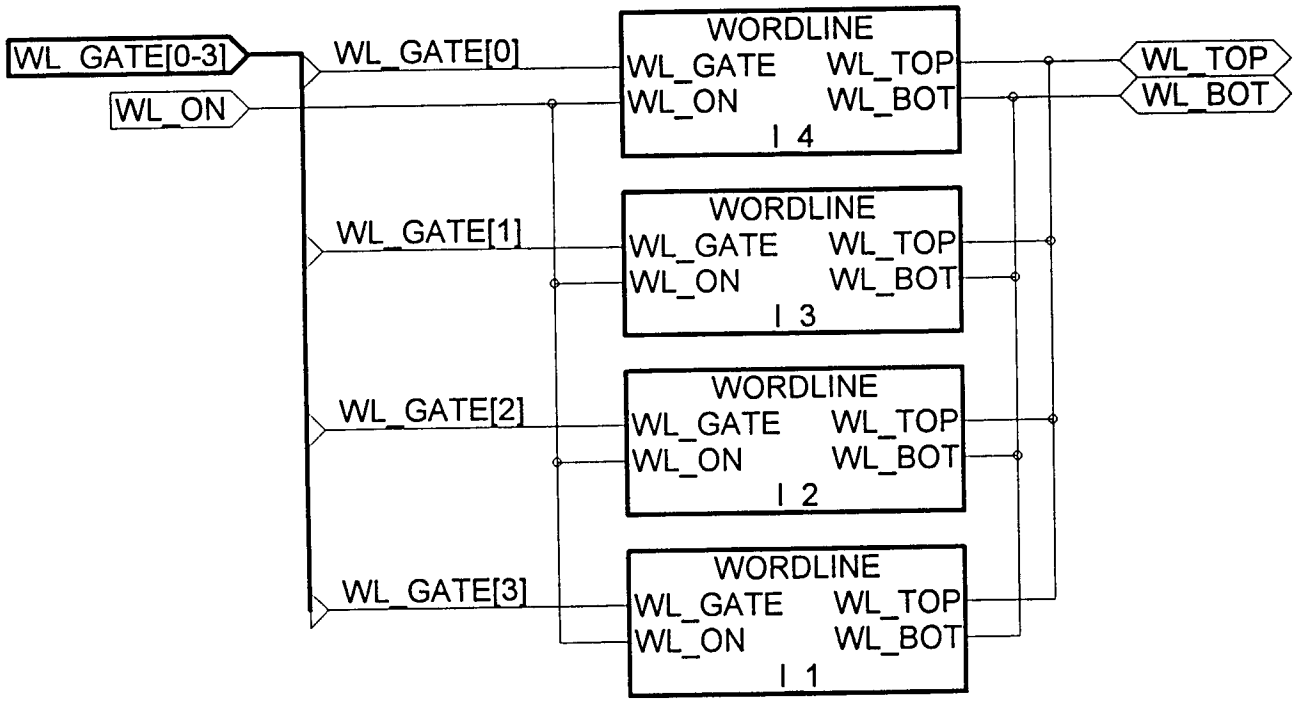

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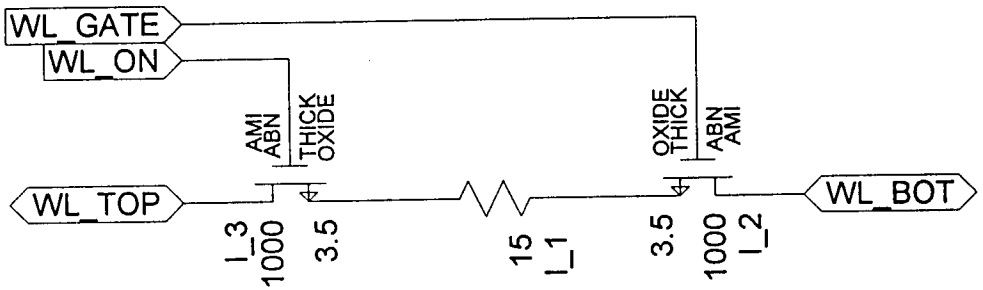

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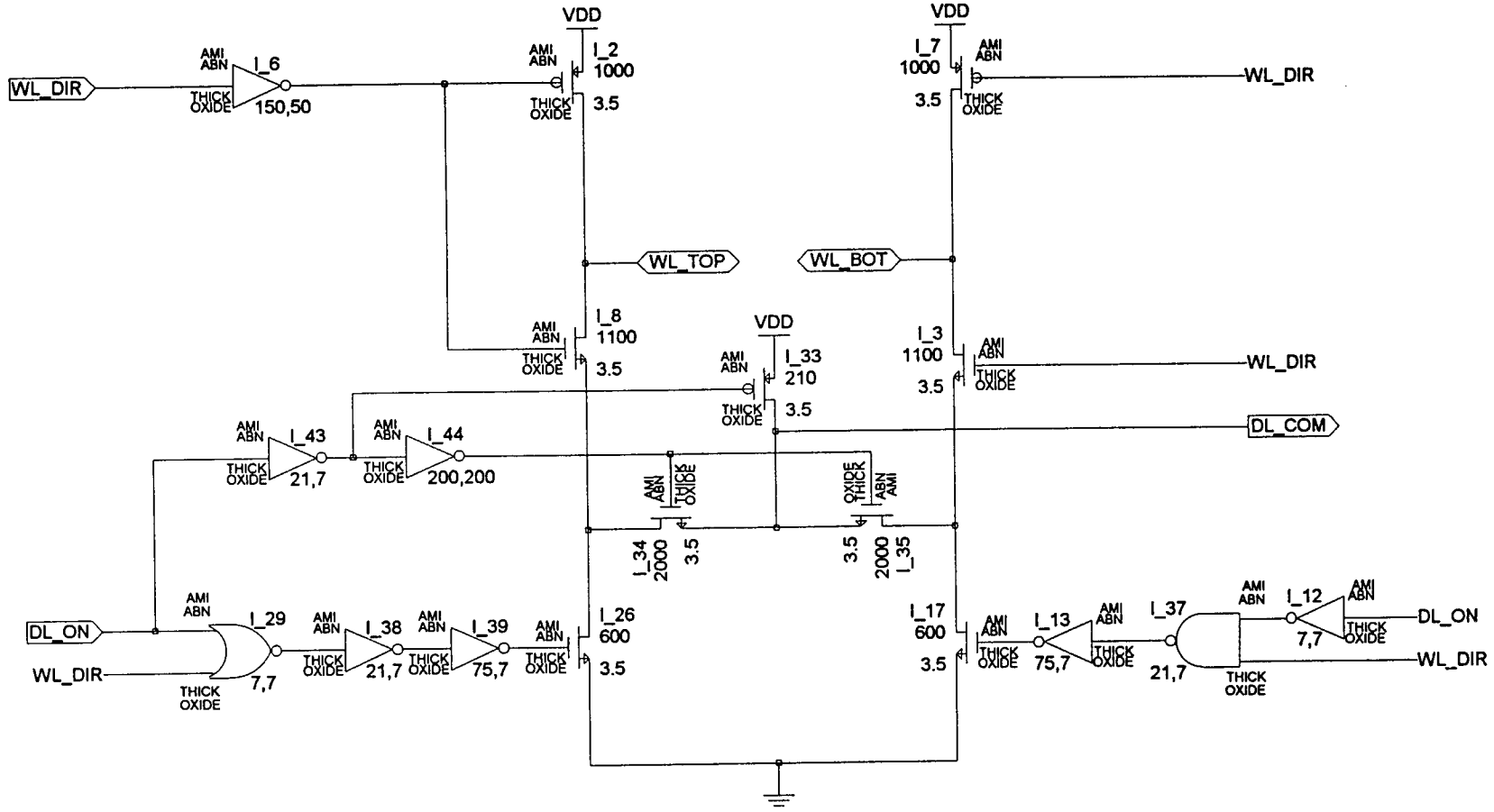

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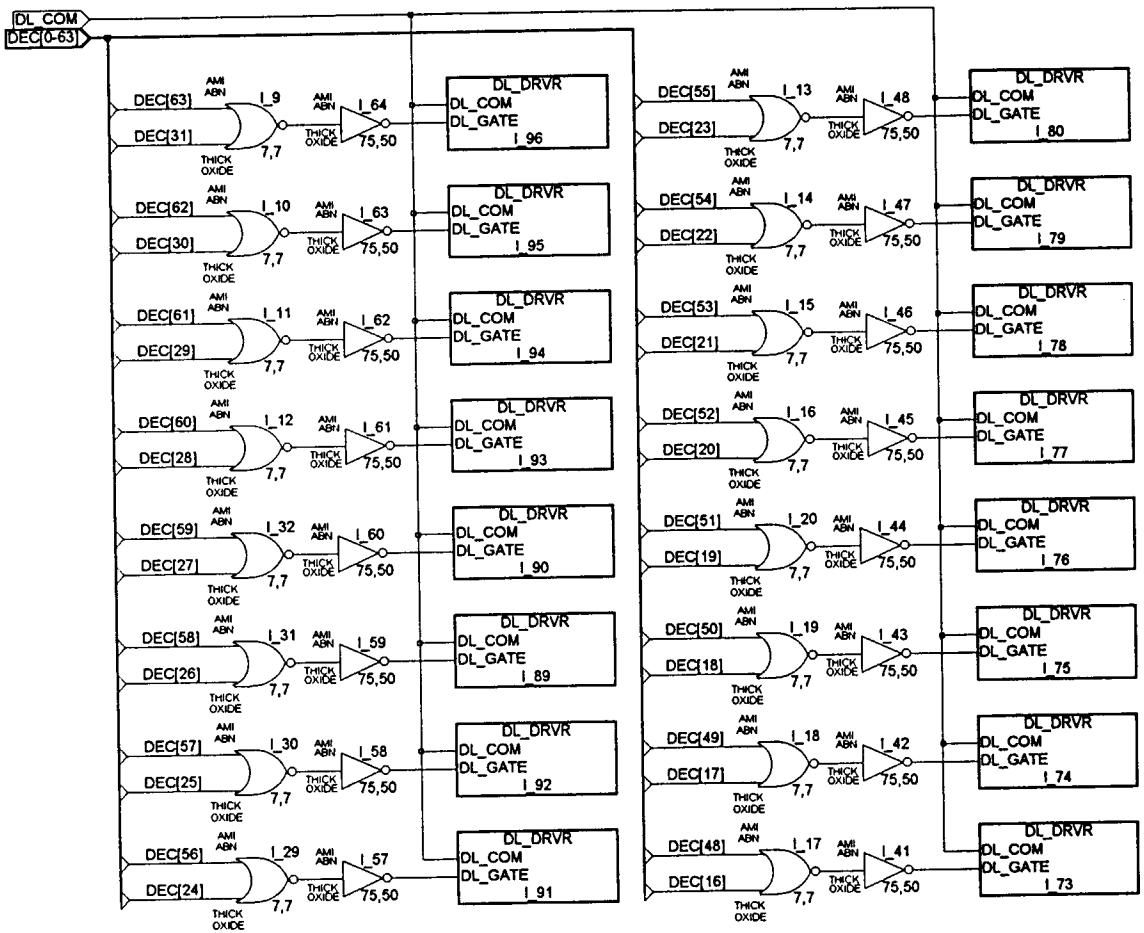

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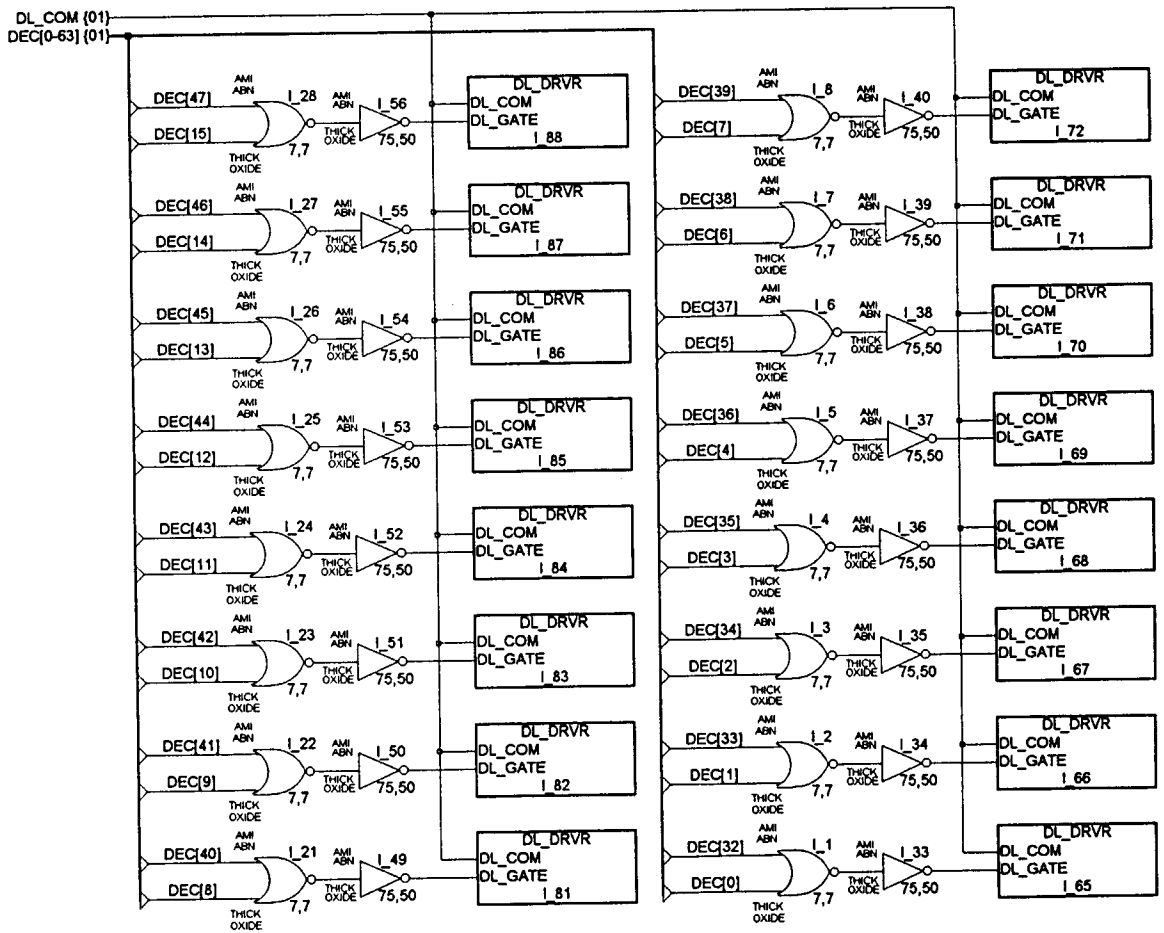

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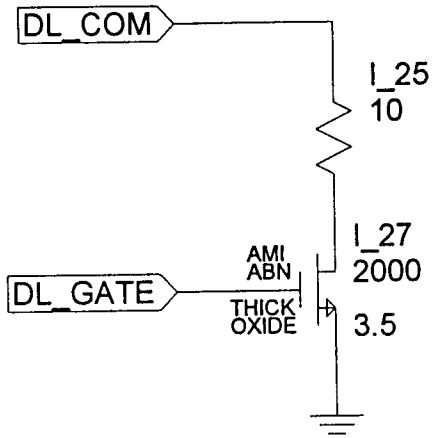

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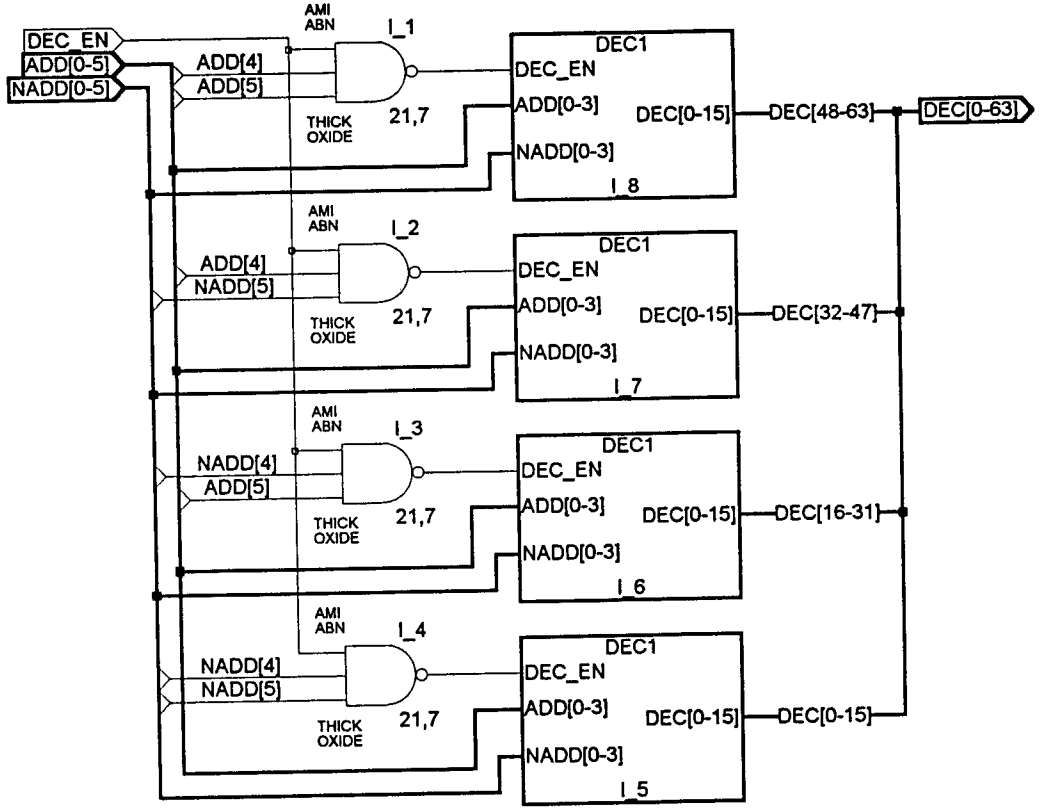

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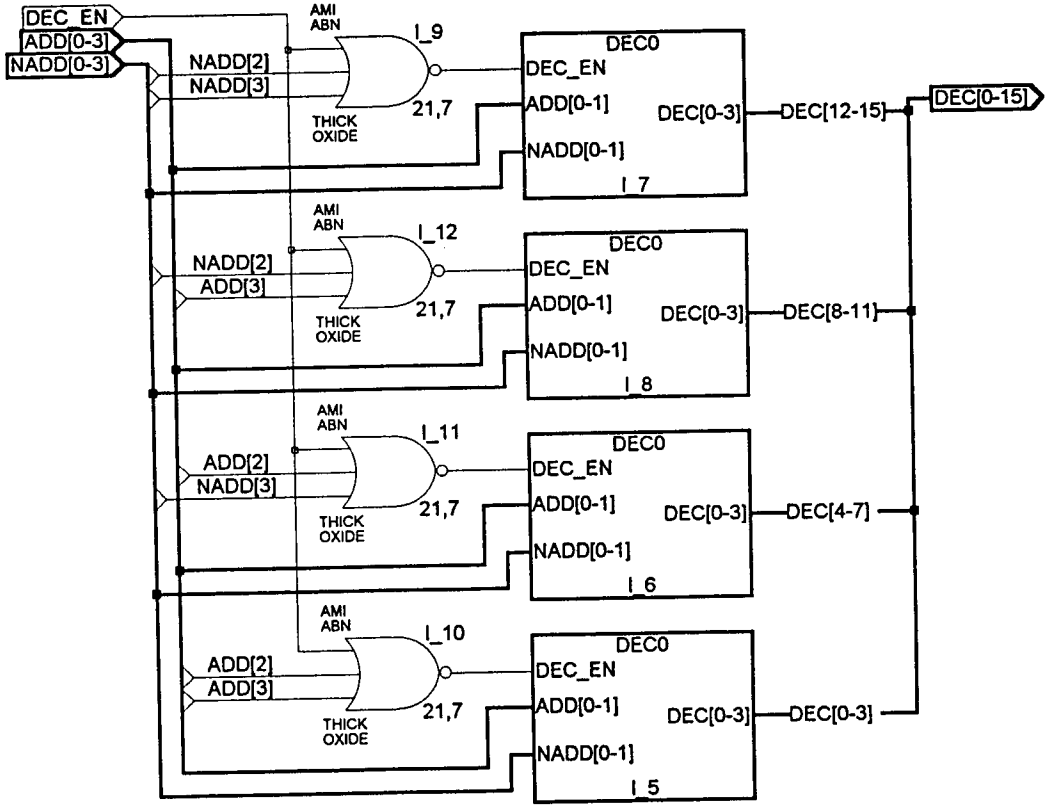

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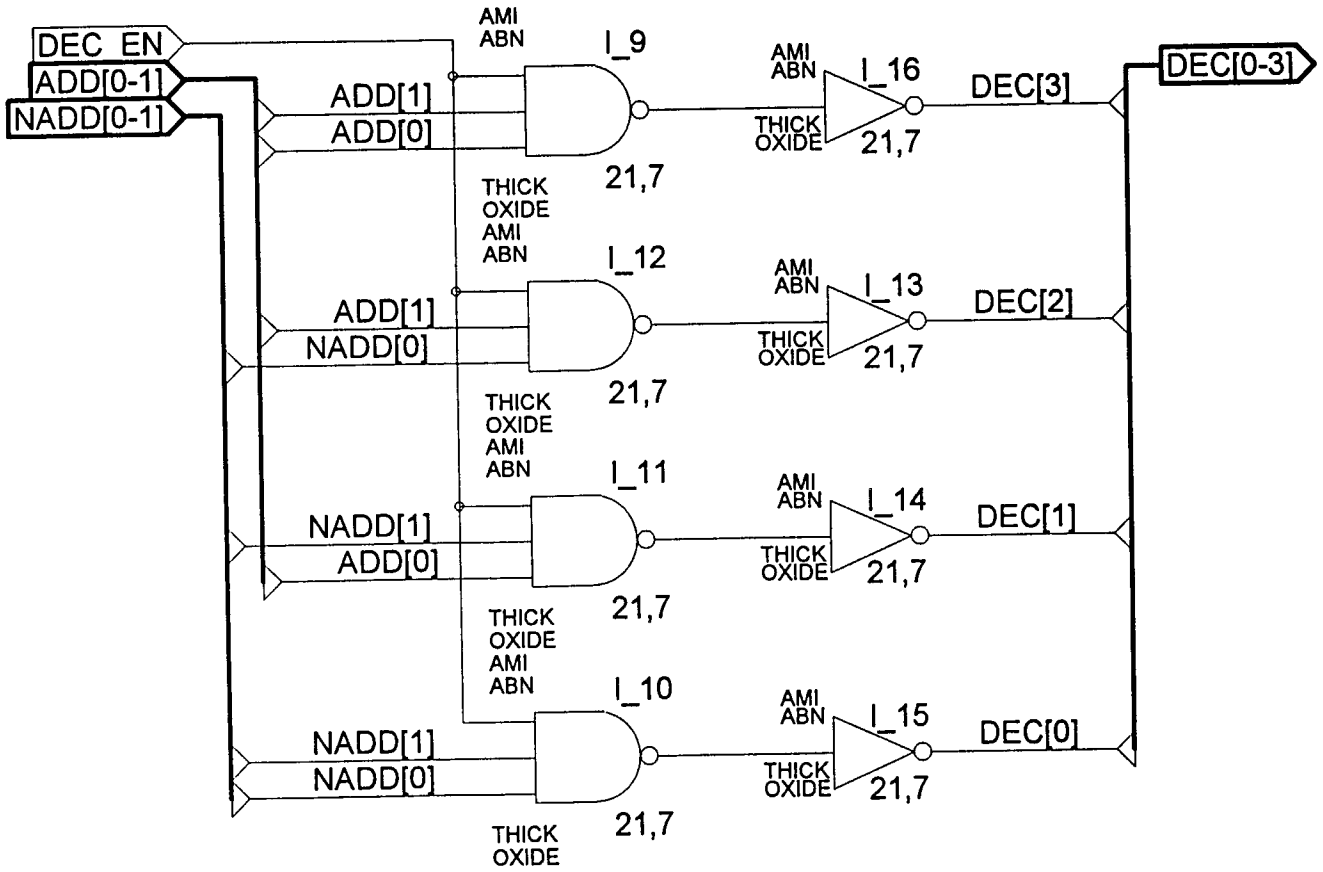

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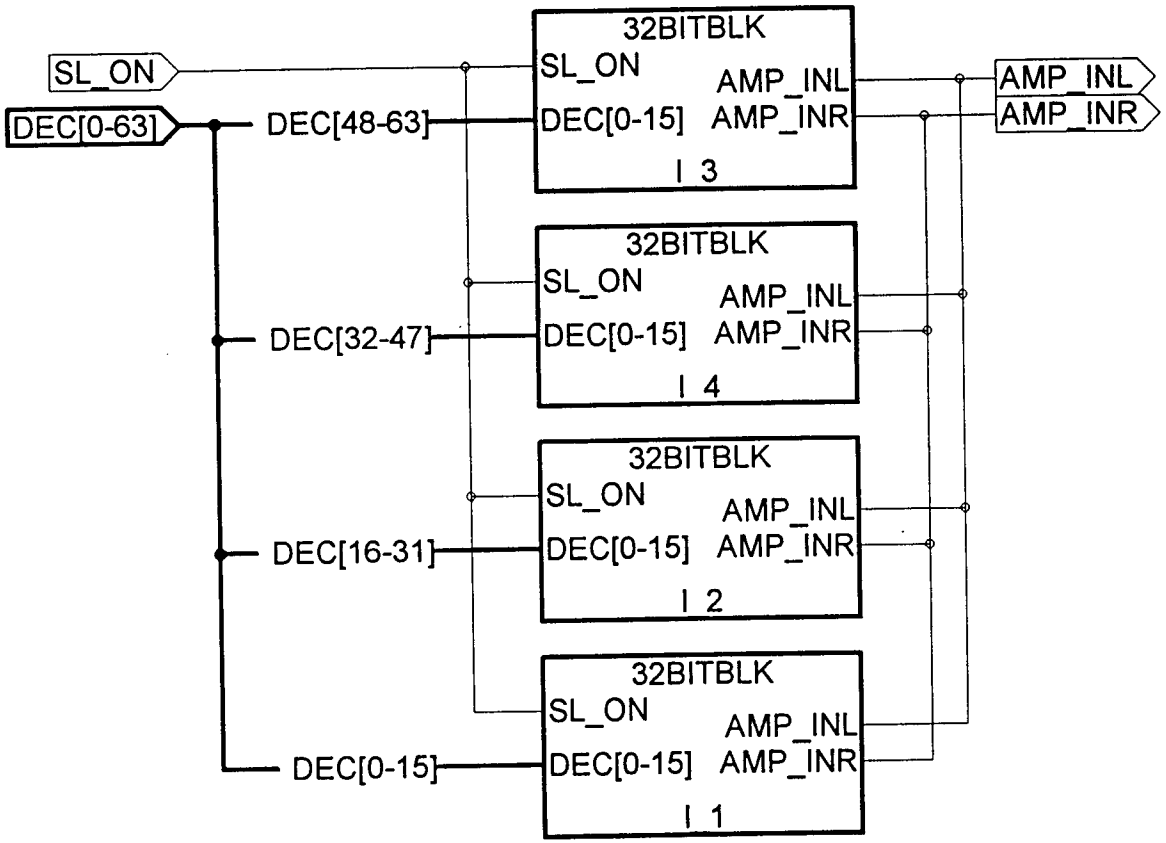

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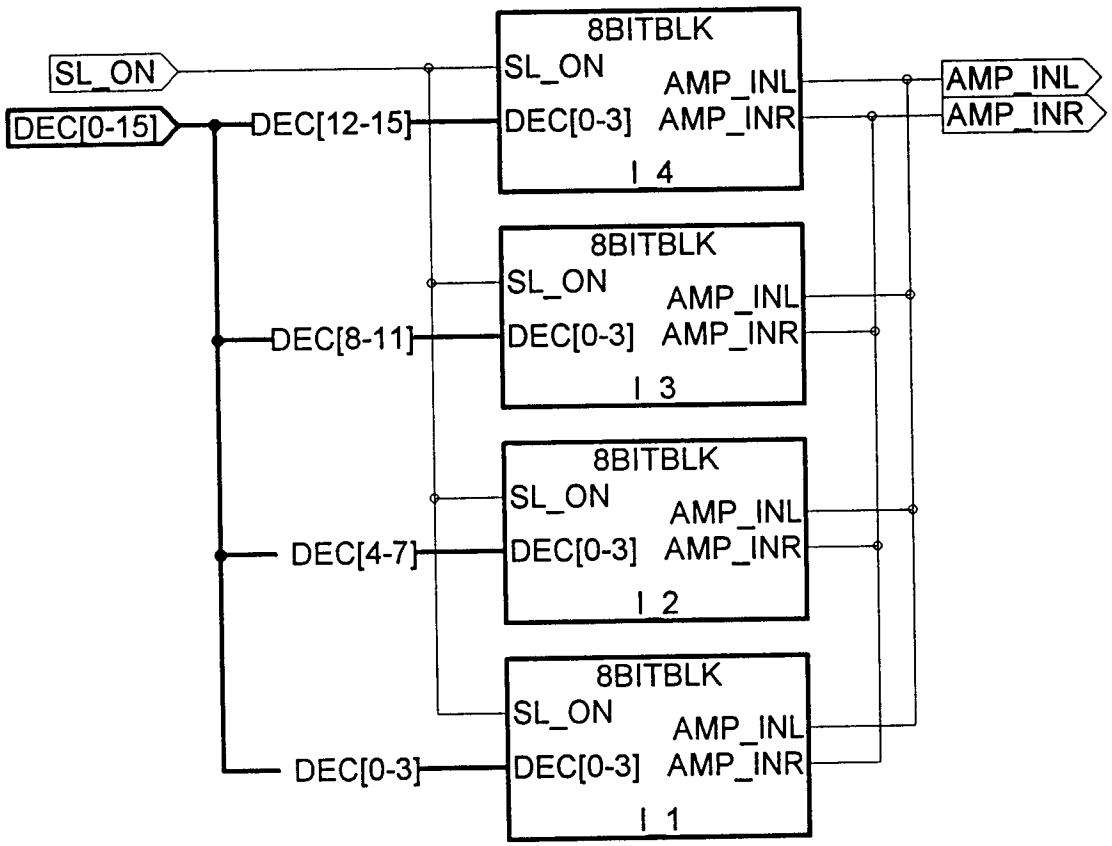

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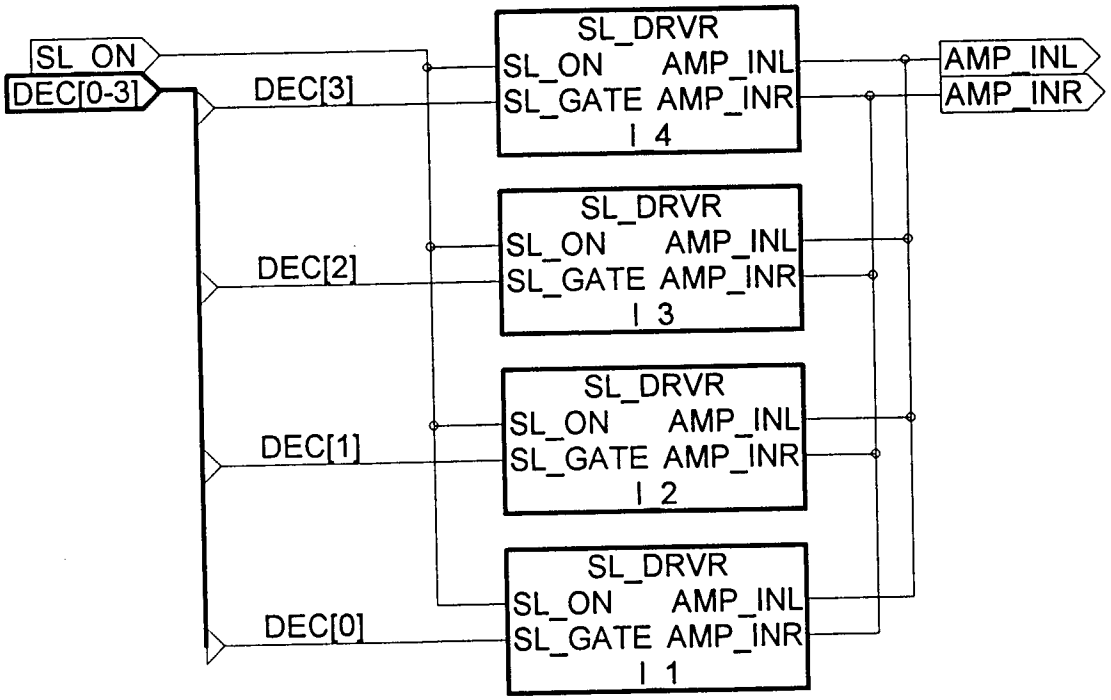

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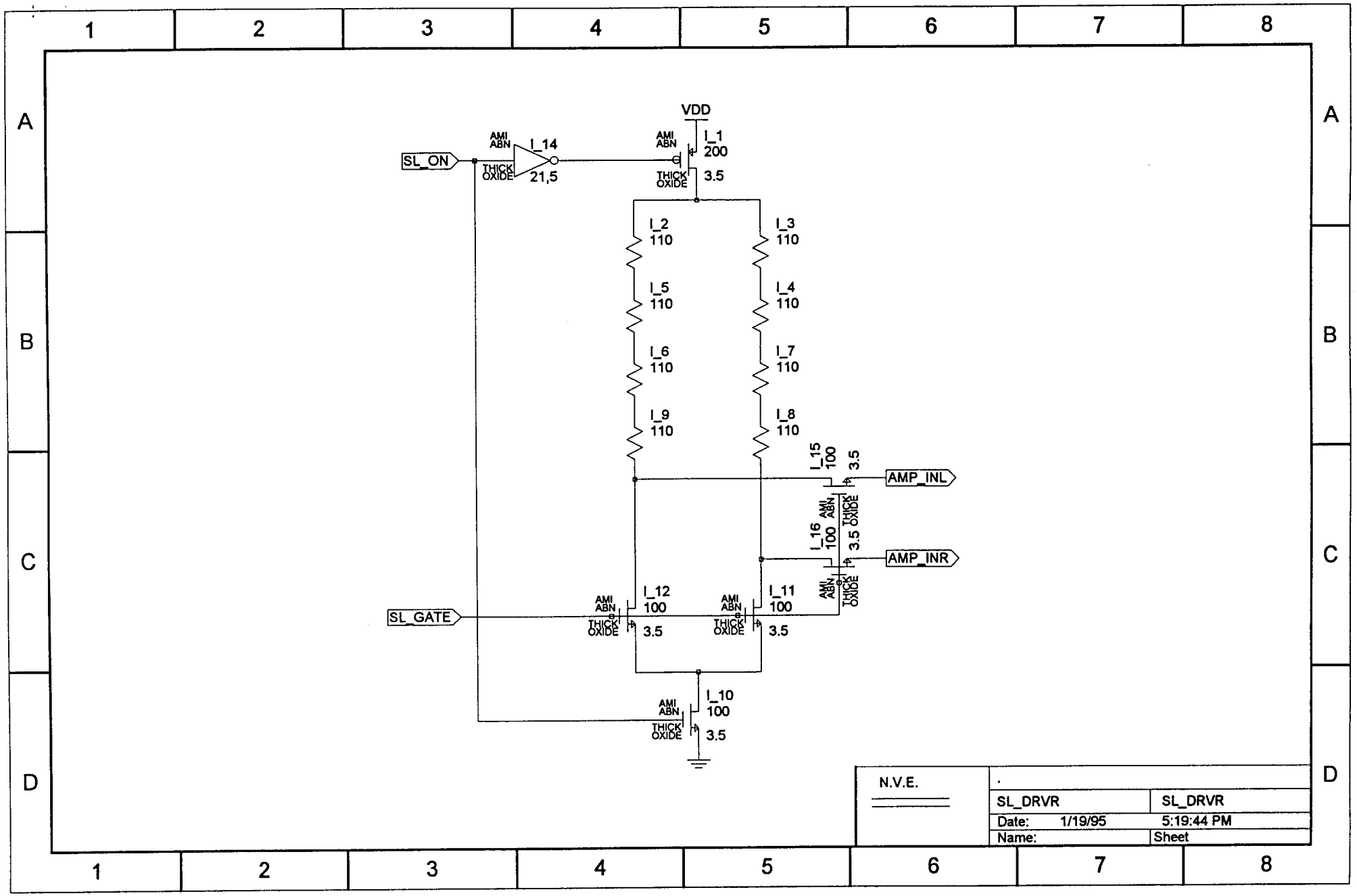
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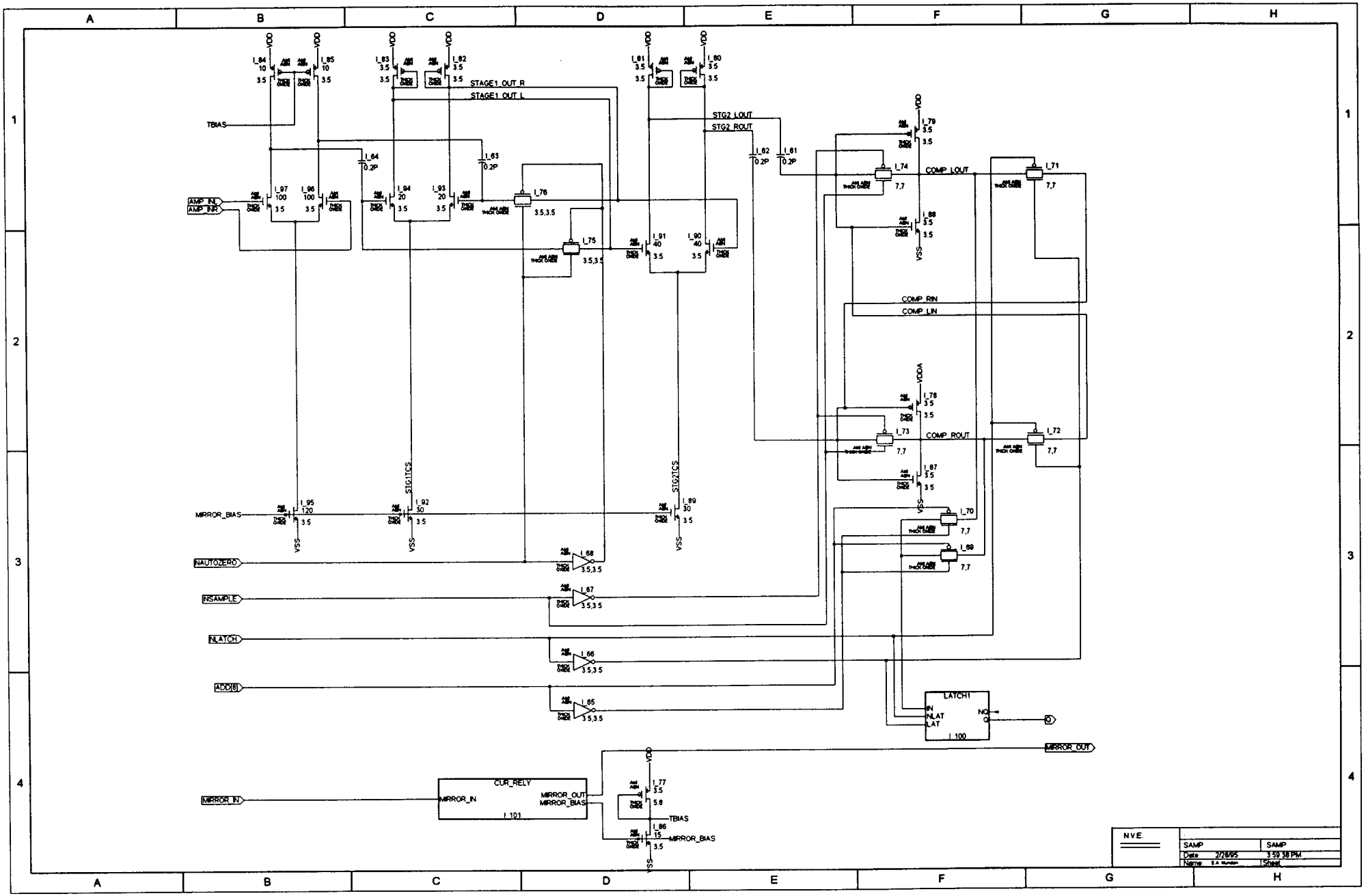
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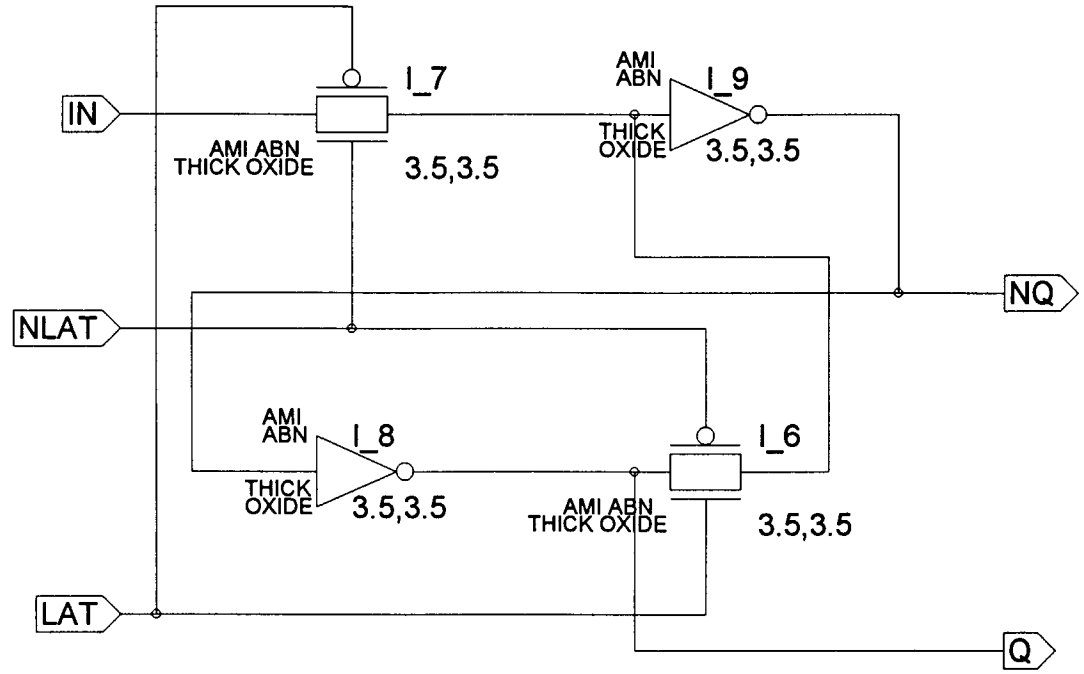

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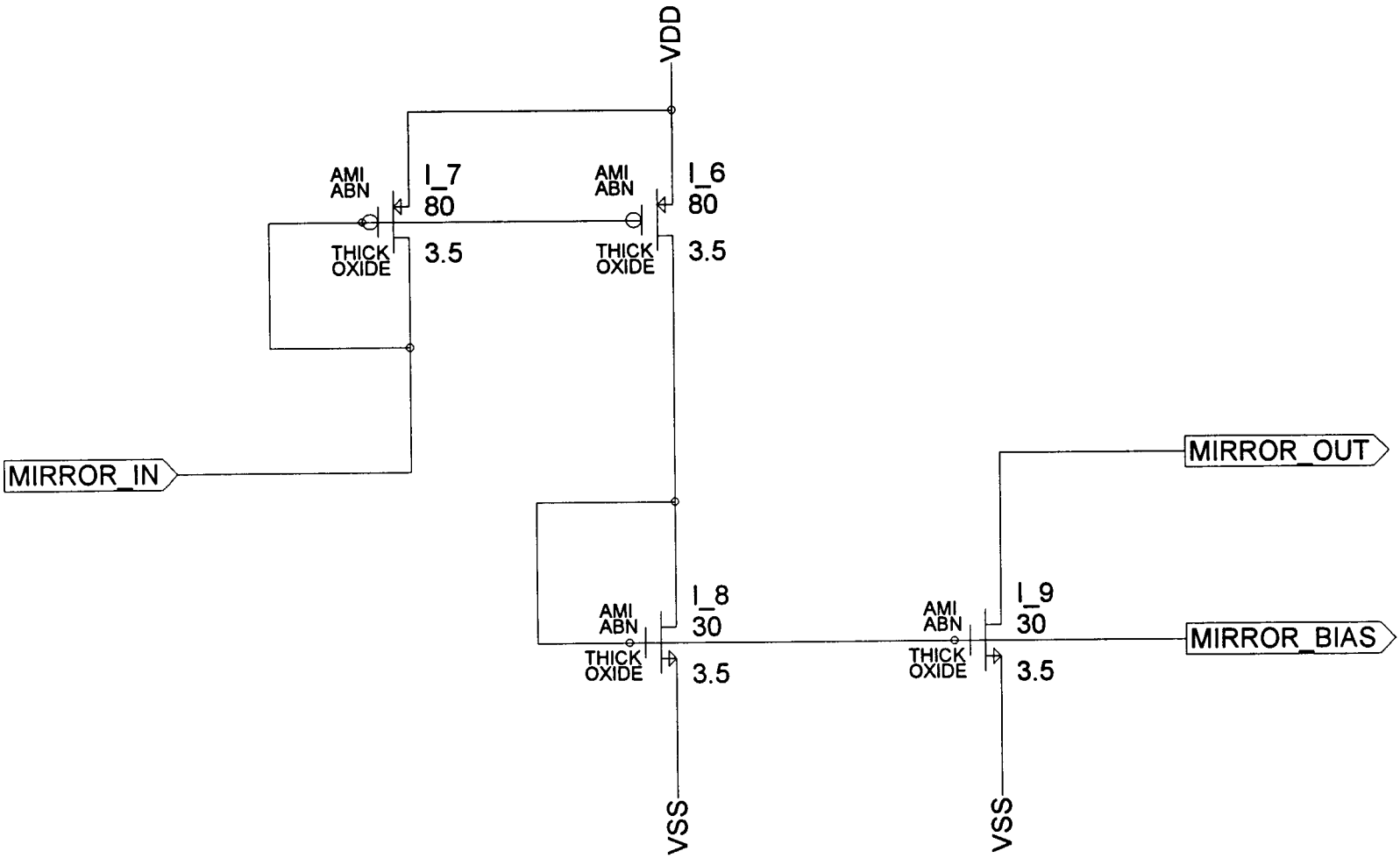

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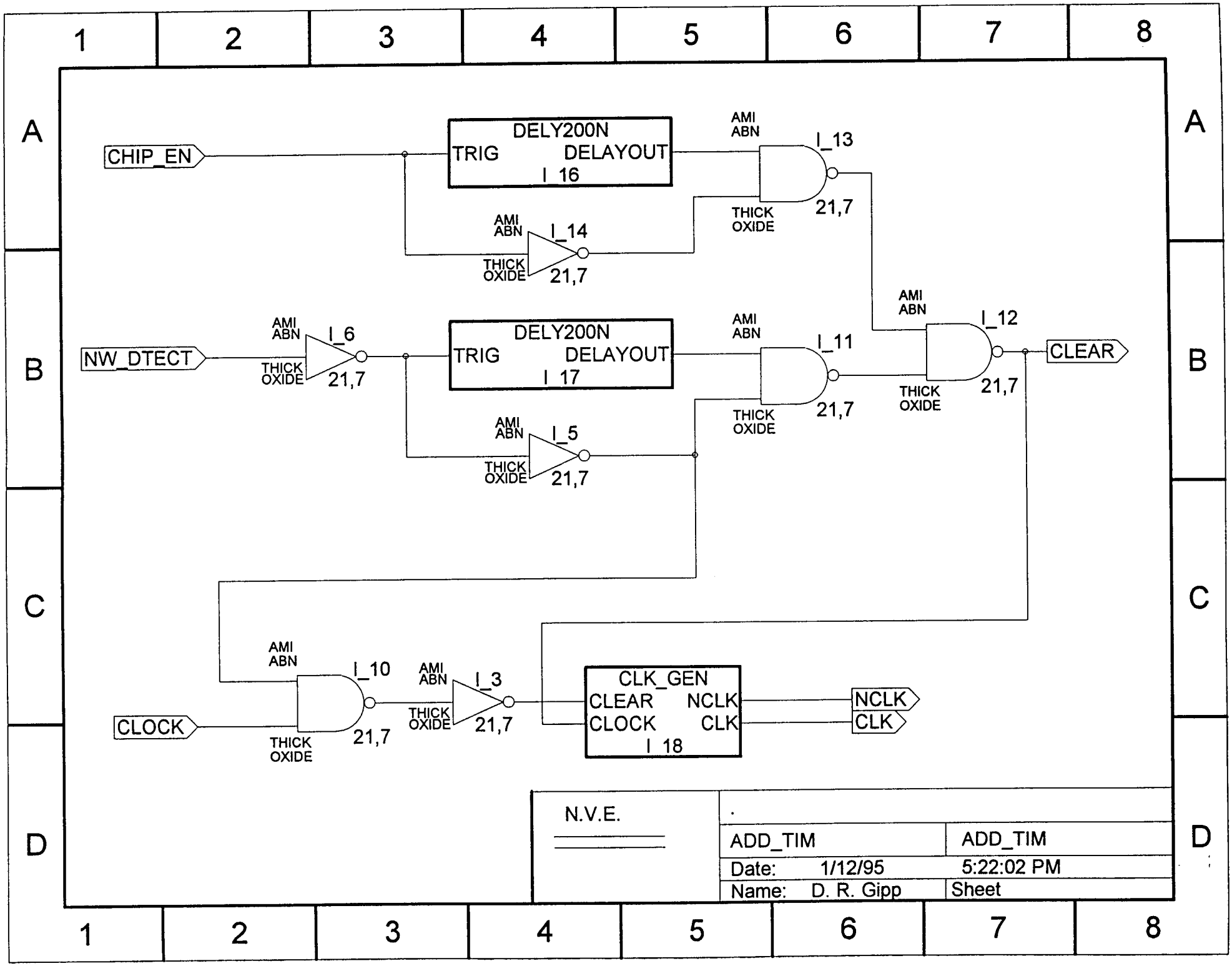
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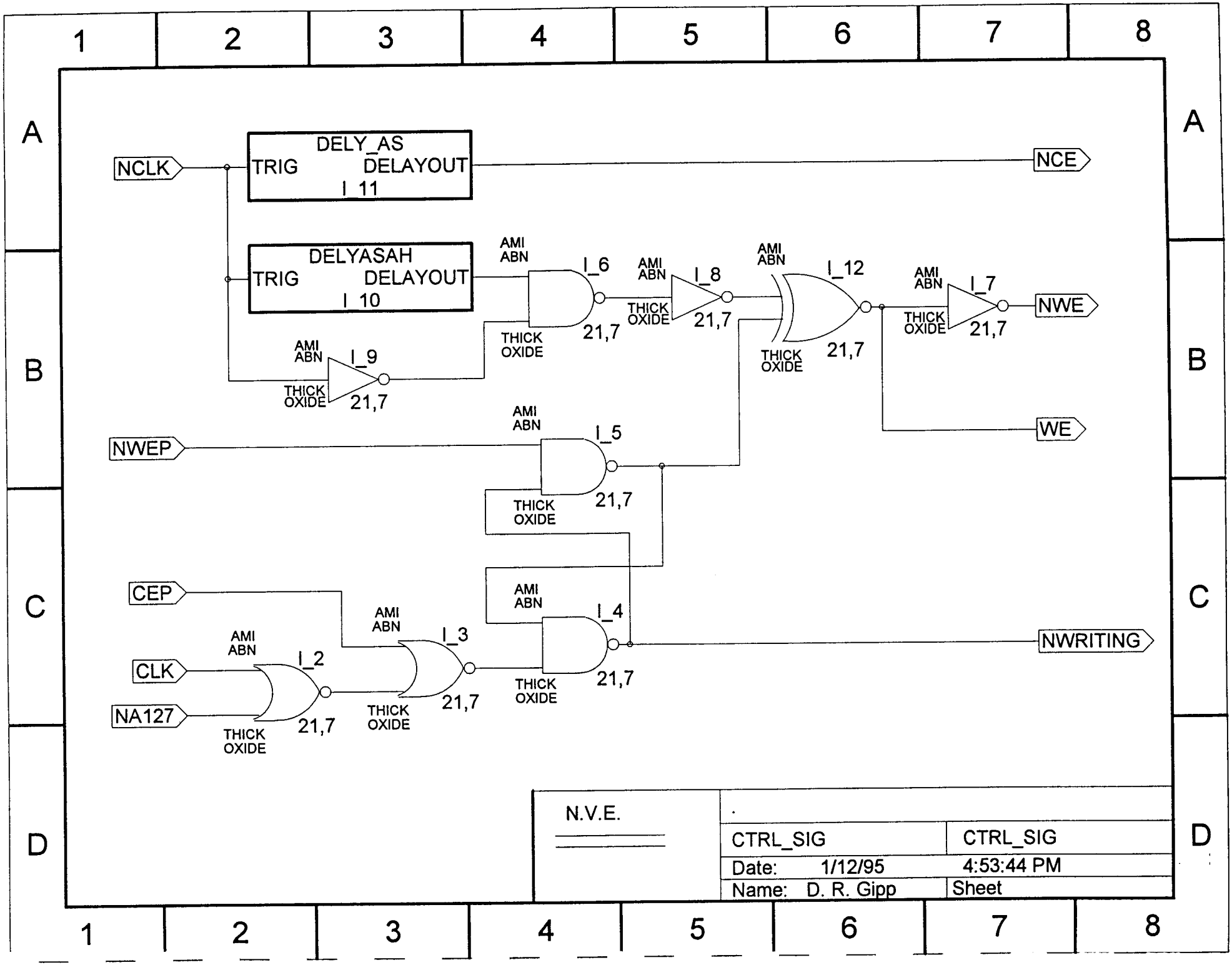
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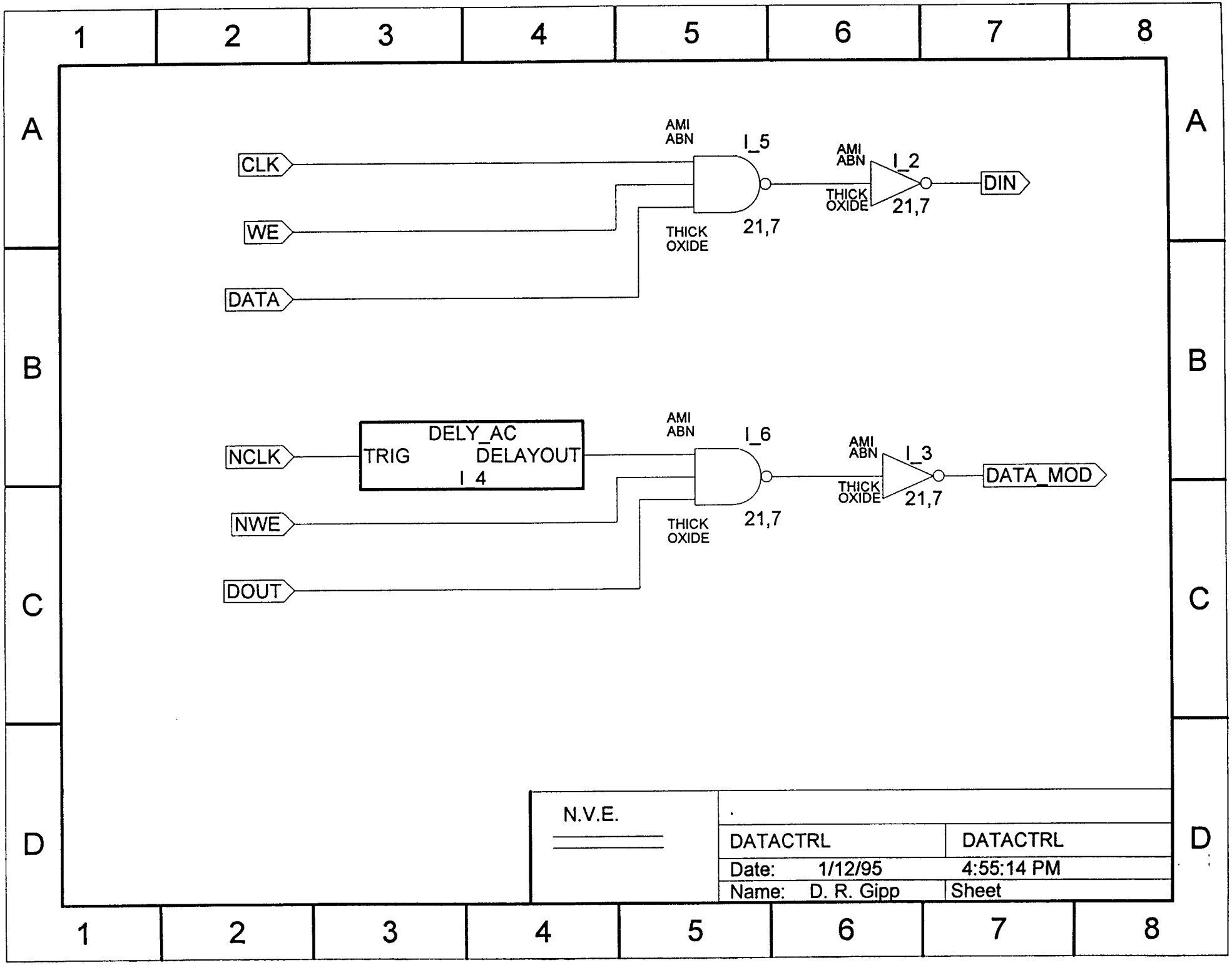
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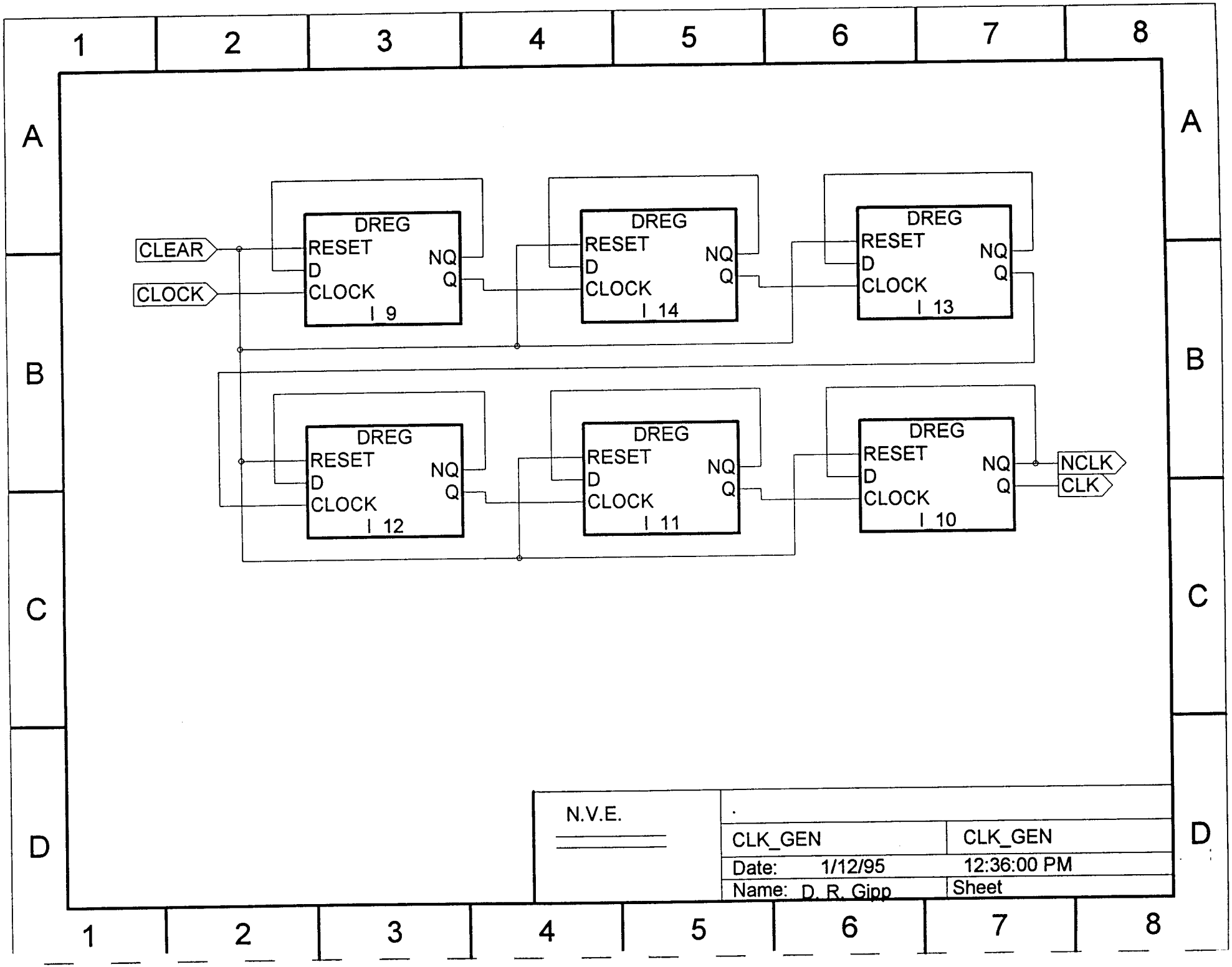
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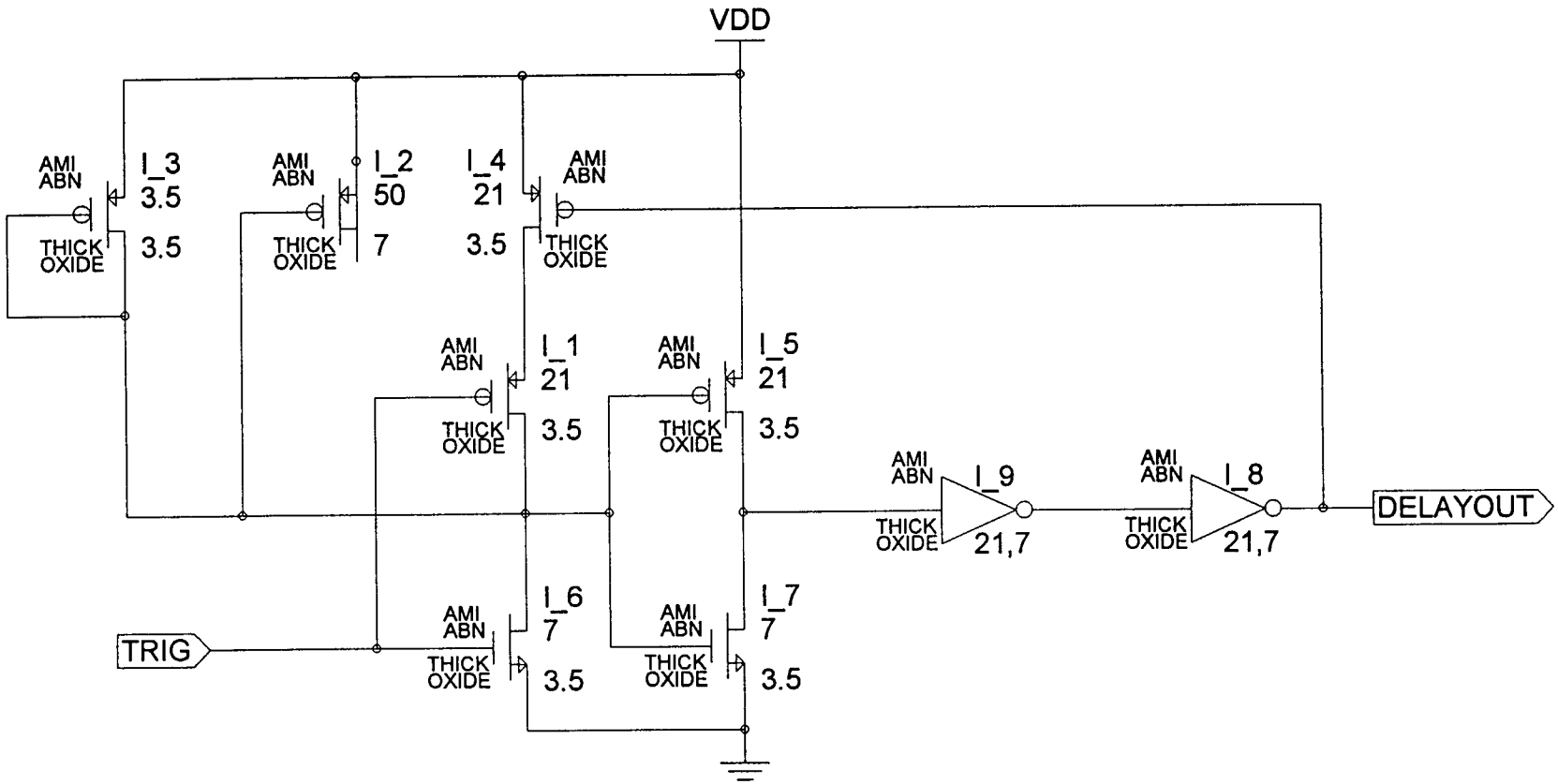

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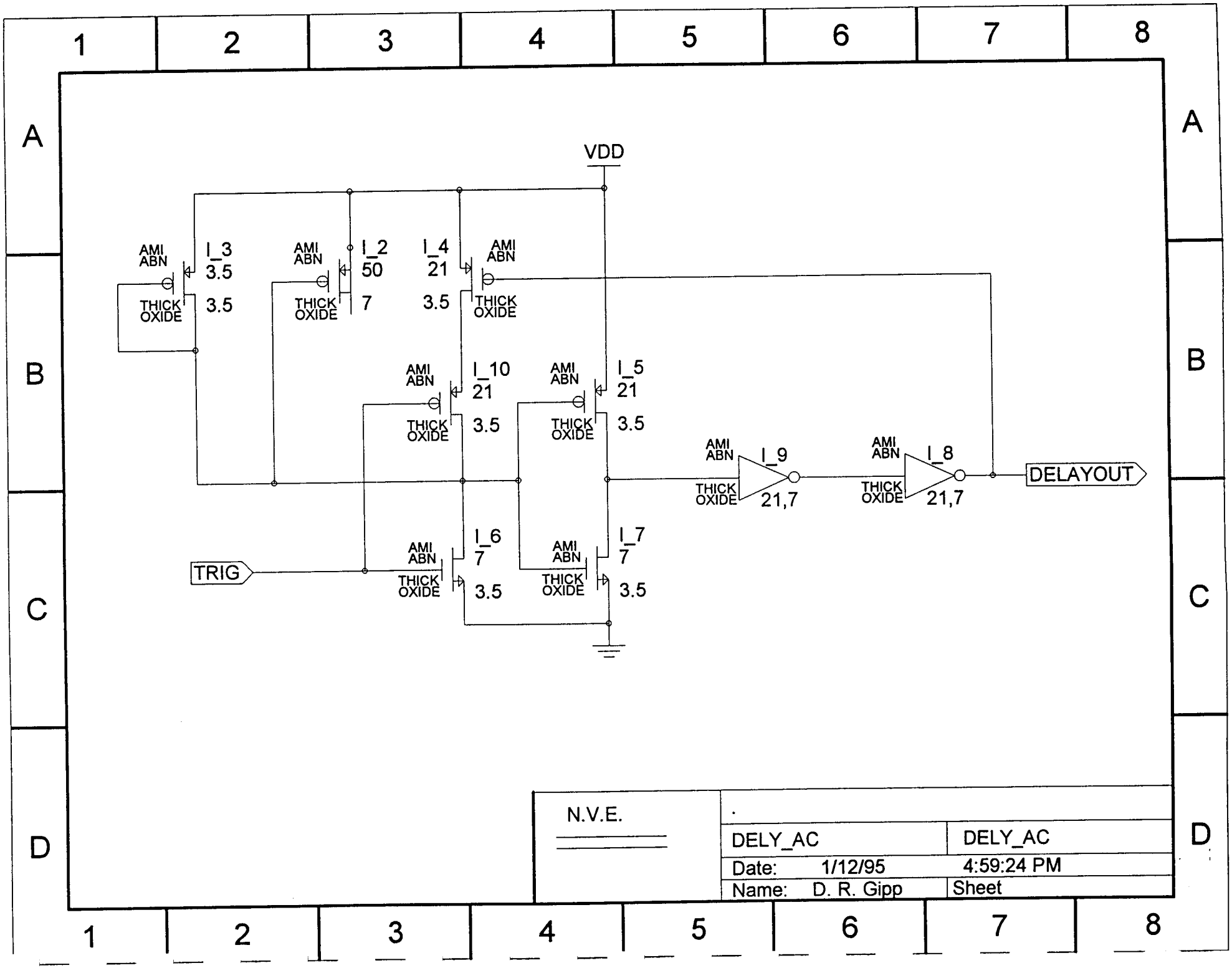
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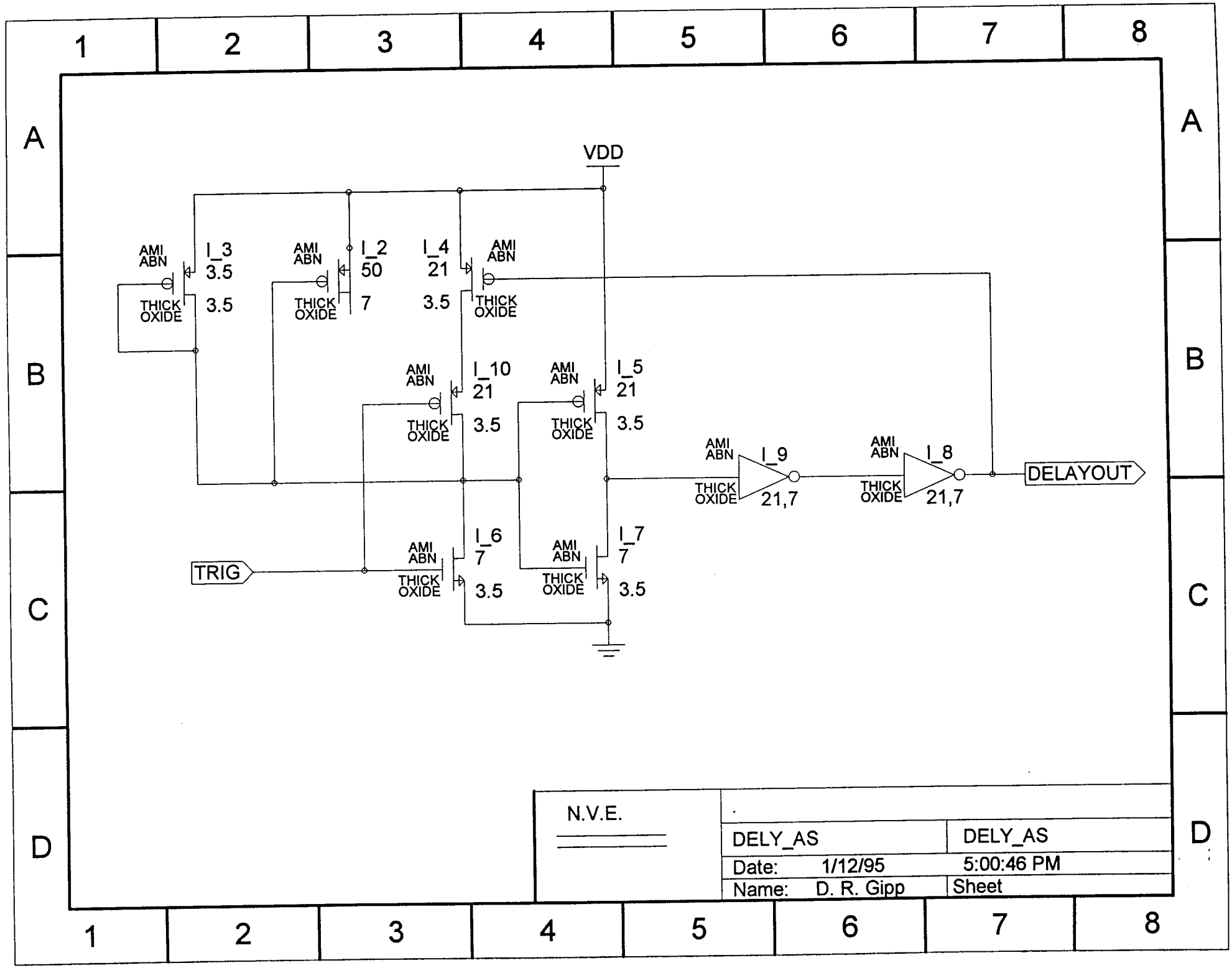
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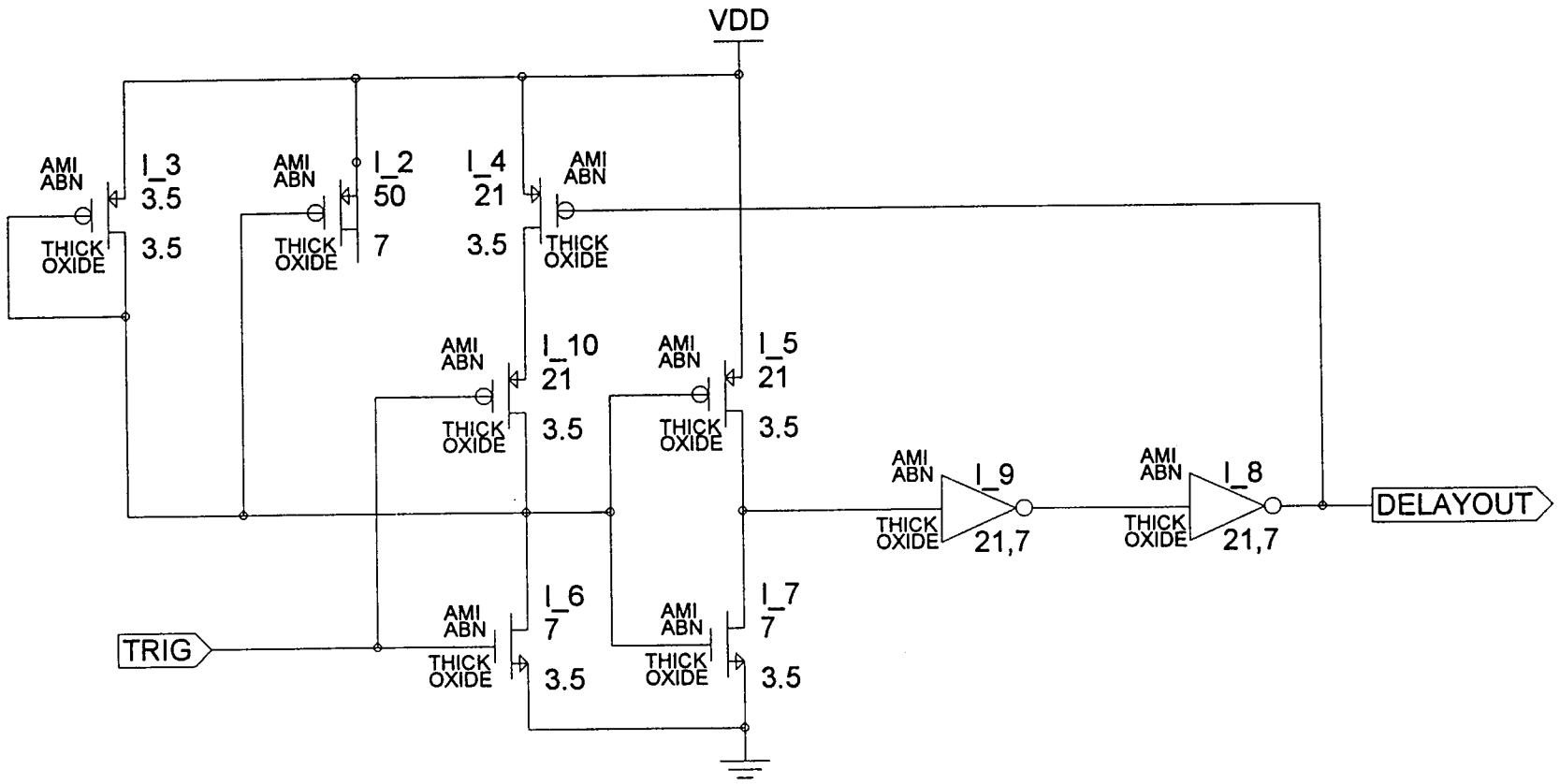

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RFID Reader Writer

(This portion of the report prepared by WJ Systems, Inc.)

Fundamentals of RFID

One needs to understand the variables and attributes of low frequency passive RFID for effective application of the technology. The strengths and weaknesses of RFID technology must be considered in a system perspective in order to optimize the final operational system.

A fundamental phenomenon of physics is that an alternating electrical field in a wire will produce an associated equivalent alternating magnetic field. When this alternating field is in the proximity of another wire, it induces a current in this second wire. This is the principal of a transformer where the electrical parameters or characteristics of voltage and current are changed to meet specific requirements. For example, electric power transmission lines are high voltage and low current to reduce the size of the transmission wires. The power line that supplies a normal household may have a voltage of 7.5K volts to the transformer. This voltage is then reduced to 120 volts and 240 volts for household use. The voltage reduction is performed by a step-down transformer that has roughly about 60 times as many turns of wire in the primary coil (7.5K volts) as in the secondary coil (120 volts).

The typical transformer consists of an iron core and two coils of wire. The iron core is shaped like a square. Around one side of the core is wound a wire known as the primary coil. Another coil is wound around the other side of the core, or in some cases around the first coil, and is known as the secondary coil. The two ends of the primary coil are connected to the source voltage. The ends of the secondary coil are connected to the circuit to which the electricity is to be transferred. As the alternating current goes through the primary coil, it sets up a magnetic field, much the same as if it were a magnet. This magnetic field consists of lines of force or flux that change in number and direction. These lines cut through the turns of the secondary coil, which

sets up an alternating current in this coil. The current in the secondary coil is known as induced current, and the voltage is known as induced voltage. The current induced is directly proportional to the number of turns in each transformer coil while the voltage is indirectly proportional to the number of coil turns. There are many types of transformers, with another being an air-core transformer which does not have an iron core. These two types of transformers are used in RFID systems.

Passive RFID consists of an active element, having a single transmitting and receiving coil in the same plane, which operates by transmitting an electromagnetic field within the proximity of a passive electrical circuit, thereby inductively coupling the coil (air-core transformer) with the passive circuit. When the passive circuit is inductively coupled with the coil, a characteristic change in the transmitted electromagnetic field occurs that can be detected by the electronics associated with the receiving coil and used to trigger some mode of operation for the system.

More sophisticated electronic systems use an exciter coil to transmit a directional electromagnetic energy field in the proximity of an electronic tag or transponder. The transponder is energized by the electrical energy inductively transferred by the transmitted magnetic field and is made operative to output a modulated identification signal which can be detected by an inductively coupled receiving coil. The passive tag or transponder element of many of these devices includes a coil which receives electromagnetic energy from a transmitted interrogation signal and re transmits an identification signal developed by the identification circuitry of the transponder. Electrical control circuitry within the transponder converts and rectifies the energy received from the coil and develops a DC power source for use in operating the transponder's identification circuitry.

As a point of discussion and the acceptance of a few aspects of electromagnetic theory, we can provide some insight into the variables relating to RFID signals. Consider that there are two elements in an RFID

system: a field source (transmitter) and a point source (transponder). Without getting into the physics of transmission fields, the field strength of the source or transmitter drops at $1/d^2$. "d" equals the distance from the face of the coil. Similarly, the field strength of the point source drops at $1/d^3$. This explains the rapid loss of field strength as the distance between the transmitter and receiver (RFID reader and transponder) increases. The sum of the two field strengths is $1/d^5$ at the RFID reader, where d is the distance between the receiving coil and the transponder coil. Early generations of RFID systems were extremely limited in signal detection. Hence, the reader needed to be placed in very close proximity to the transponder in order to detect the identification signal. This limitation greatly restricts the utility of such devices, since not all objects may be so closely approached in order to be read. These devices are also highly susceptible to interference and noise produced from other sources, which affects the integrity of the detection part of the system. This problem increases in severity as the transponder is moved away from the interrogator, since it becomes more and more difficult to distinguish the low intensity transponder field from extraneous noise as the transponder field drops in strength.

The objectives of an RFID system that provides for optimal performance are:

- an electromagnetic field transmission and detection system which can simultaneously transmit a directional magnetic field and detect a localized low intensity magnetic field

- an electromagnetic field transmission and detection system which can accurately detect a localized low intensity magnetic field in the presence of a higher intensity magnetic field or other uniform electromagnetic interference

- an electromagnetic field transmission and detection system which is capable of accurately detecting very low energy magnetic fields from the low energy transmission source

There are a number of technical trade-offs that can be made for RFID systems to aid in the optimization of electromagnetic field transmission and detection.

Two key areas of trade-off are the transmission mode and the signal detection mode.

The transmission mode can be either full duplex or half duplex. The full duplex mode is one where the transmitter generates a constant signal to the receiver (transponder), and the receiver (transponder) returns a constant signal as long as the transmitter is providing power. This type of RFID system uses a tuned antenna in the transponder that provides current and voltage to power the transponder in a constant transmission state. The half duplex mode is one in which only one device transmits at a time. The transmitter transmits a signal for a predetermined length of time that charges a capacitor that will power the transponder. When the transmitter turns off, the capacitor discharges to the transponder circuit, providing the power for the transponder to transmit back the data in the transponder register or memory. Including a capacitor as part of the transponder circuitry is not a problem with large transponders. An overall size problem occurs when adding a capacitor in designs such as the integrated MRAM transponder.

The trade-offs in signal transmission are amplitude and sideband or pulse width modulation schemes to detect the occurrence of a binary 1 or 0. Other schemes exist, but require greater complexity to generate and decode. In order to minimize the transponder circuitry, and therefore its power consumption, the more complex methods are not desirable. Another consideration is the need for a continuous field to power the transponder while it is transmitting data. Methods such as amplitude and sideband, or pulse width modulation reduce the transmitted power during the modulation process and will therefore reduce the power available for the transponder operation.

Preferred Technical Approach

As a developer of custom RFID systems, W. J. Systems has experience with various system design alternatives. We propose that a full duplex phase shift design will optimize the system to obtain maximum signal detection in both range and for operation in challenging background signal environments.

This system transmit antenna will operate full duplex at a frequency optimized with the characteristics of the transponder design. The receive

antennas will operate at exactly one-half the transmitter antenna. There is an inherent benefit in using this approach. The transponder receives power and clock from the magnetic field that the transmitter generates. The transponder antenna voltage will amplitude modulate at one-half of the transmitter frequency. The one-half exciter frequency as a sub carrier will allow for a high data transmission rate and produce the highest usable re-radiated energy.

An inherent phenomenon which should be of no surprise to anyone is the effect of most metals in the proximity of RFID systems. The metal effectively detunes the transponder coil significantly which drops the read range. Most RFID systems operate at a fixed frequency and as a result, many systems cannot read a transponder in this environment. Our system design avoids some of the effect by slightly shifting the transmitter frequency to compensate for the detuning of the transponder signal. The frequency shift is a result of metal "detuning". The frequency at the receiver is at one-half the transmitter frequency. We estimate that the system frequency will be able to drift about 5% to compensate for signal shift which means that the read frequency will operate over a broader frequency range. The result will be highly sensitive electromagnetic receiver electronics that are less susceptible to interference than the single or dual coil RFID designs that operate at a fixed frequency.

Planned System Overview

The planned representative RFID system will consist of a Reader/Writer and multiple transponders. The reader will transmit a directional alternating magnetic field to power the transponders.

The Reader/Writer is a computer processor system that controls the functions relating to powering the transponder and processing the return signal from the transponder which contains the stored information.

The initial form-factor of the Reader/Writer will be panel type module packaged in a standard electronics enclosure for flexibility in implementation and packaging. The control electronics will also be packaged in a similar

manner in a standard electronics enclosure. The Reader/Writer interface with a computer via an RS-232 serial channel to input data into the transponder. A Liquid Crystal Display (LCD) on the control electronics module will display transaction information such as the data to be stored or data that has been stored in a transponder.

Reader Operating Mode

The reader will have two light emitting diodes to provide the operator with a visual indication of the reader status. A red light will indicate read mode while a green light will indicate the read of a transponder. An audio speaker will also provide an indication of reader operation. A high pitched tone will emit whenever a transponder is read. This eliminates the need to look at the indicator lights.

Reader/Writer System Architecture

The Reader/Writer will consist of an exciter to power the transponder for both the read and write function as shown in Attachment A. A receiver circuit amplifies and limits the transponder signal for both functions. The exciter will drive the exciter antenna with a AC current. The resulting magnetic field will power the transponder as previously described. The differential receiver collects the modulated signal emitted by the transponder. The receiver circuit will consist of bandpass and notch filters, low-noise amplification, and limiting stages to recover the phase modulated sub carrier from the antennas. The recovered signal will be applied to a comparator which "squares up" the sinusoidal receiver output for application to the phase detector flip flop. The received signal is synchronous with (but not necessarily in phase with) the excitation current to allow an easy trigger of the phase detector. This will recover the changes in phase of the incoming signal. The microprocessor will log phase changes and extract the correct identification code using multiple code transmissions and detection algorithm.

Reader/Writer Operation

After stimulation by the exciter field, the transponder signal is sensed and amplified by the receiver gain and filter stages. The receiver output is further limited by a comparator, and phase demodulated. The microprocessor extracts the identification number from the incoming signal using suitable algorithms. In addition, the processor controls the power distribution to other system blocks, drives an LCD display and speaker, monitors actuation of the read or write cycle initiation, and implements an RS-232 interface. Reset logic allows a manual actuation as well as a connection to the RS-232 port to reset the microprocessor.

Read Cycle

The exciter produces an alternating magnetic field that inductively couples with the transponder during the read cycle. The magnetic field that excites the transponder results in a serial stream of modulated data transmitted by a similar alternating magnetic field inductively coupled with the receive antennas. The signal is converted from analog to digital for processing. The incoming data stream at the output of the detector is shifted into the microprocessor and an internal counter interrupts the processor after the shift register contains the serial information. Upon being interrupted, the processor decodes the data and compares it with the last stored word in the shift register. The result is a byte that is stored in processor memory. (Attachment B)

Attachment C shows the transponder read cycle in more detail. The reader interrogates the transponder several time to avoid errors due to noise, weak signal, or other environmental conditions that affect the read cycle. The check for valid data represents a valid bit stream with proper baud rate and framing information indicating that a transponder is in the field. Actual data decoding and integrity is determined after this process.

Write Cycle

During a transponder write cycle, the microprocessor energizes the excite antenna a second time and modulates the excite antenna with the write data for the transponder. The processor controls the exciter on/off command so

that the write data is not clipped or disrupted. After the power oscillator drive stabilizes, the transponder will accept data. At this time, the processor modulates the oscillator driving the exciter antenna with the write information.

The Functional Flow Chart (Attachment B) shows the read, write, and display process. The reader must detect a valid transponder before it will initiate a write function. A number of alternatives for the write function are possible to include password or unique codes that provide security. The writer display will always prompt the operator for information will shows status of the function during the read or write operation.

Verification of the write data is a comparison process. The data written into the transponder will be read back and compared to the data transmitted. An error will initiate another write cycle. The number of retrys is a parameter of the control software and is optimized to the operational environment.

Logic Schematic Description

The reader/writer for the RFID transponder has a microprocessor, discrete logic, a keyboard interface for alphanumeric input, a display, a power oscillator, and a read input amplifier. The read, write, and display functions are controlled by the microprocessor.

The read cycle begins when initialized by external operation such as keyboard entry or read switch initiation (Attachment E). The reader could also operate in a constant read mode for some applications. The "read" switch commands the reader to read and display any valid transponder code detected in the reader field. If the operator enters a new number before operating the "read" switch, the reader displays the present number and queries the operator for making a change. A "Yes" sends the new information to the transponder RAM and completes the message test. After a successful verification of the new data, the reader displays a "successful write" message.

The transmitting coil supplies energy to the transponder as it sends the data. The multi-stage filter circuit processes the transponder return data which is then routed to the synchronizer and the microprocessor. The microprocessor

decodes the data, checks the security, and displays the transponder ID number.

If the operator has entered a new number to program the transponder, the microprocessor introduces the data modulation into the transmitting coil circuit after comparing the security to verify that it is permissible to perform a write operation.

The microprocessor controls power supply to the various parts of the reader circuit and operates two LED indicators and an audible indicator. These indicators show the progress of the read and program operation. A feedback circuit controls the transmitter write current providing constant power to the transponder. The microprocessor also has an RS232 control port over which the reader may be operated. An external computer can cause the read operation and set up a new write data function with the proper password for remote operation.

Data Format Description

The initial transponder configuration will contain 128 bits; 64 bits which are data. We will seriously consider a standard data format such as the ISO standard now in process. A standard such as ISO will provide for broader application and implementation.

Software Overview

We propose to use an existing industry standard microprocessor for the Reader/Writer control functions. The most likely candidates will be those similar to the Intel x86 series and the Motorola x80 series. The selection of such a control microprocessor will provide flexibility for tradeoffs in implementation. These tradeoffs are those functions such as decoding the identification numbers of the transponders read, control the write sequence of the transponder data, control data transfer on the RS-232 port, and execution of test routines.

Attachment D is the reader software timing diagram. It shows the interaction of the various software modules and approximate time duration relationships.

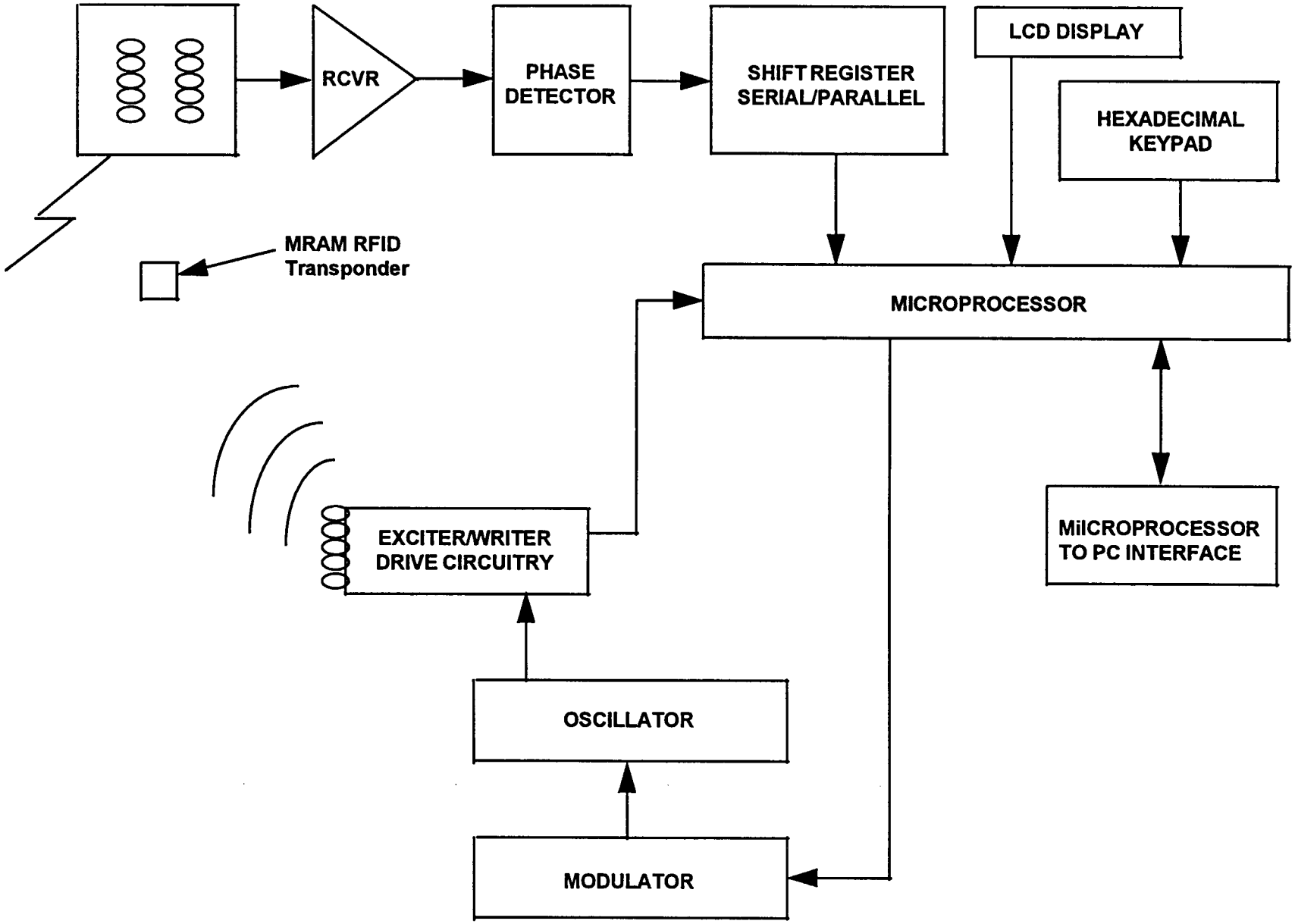
The top sequence shows the activity when a cycle is initiated.

The second line shows the read and write sequence. The write cycle does not function unless the operator enters new data for the transponder (refer to Attachment B for this sequence).

The bottom line shows the cycle completion when the microprocessor indicates the successful completion of a cycle, displays the number of a tag or status, and returns to a power condition.

A size C schematic of the reader/writer circuit is included at the end of this report.

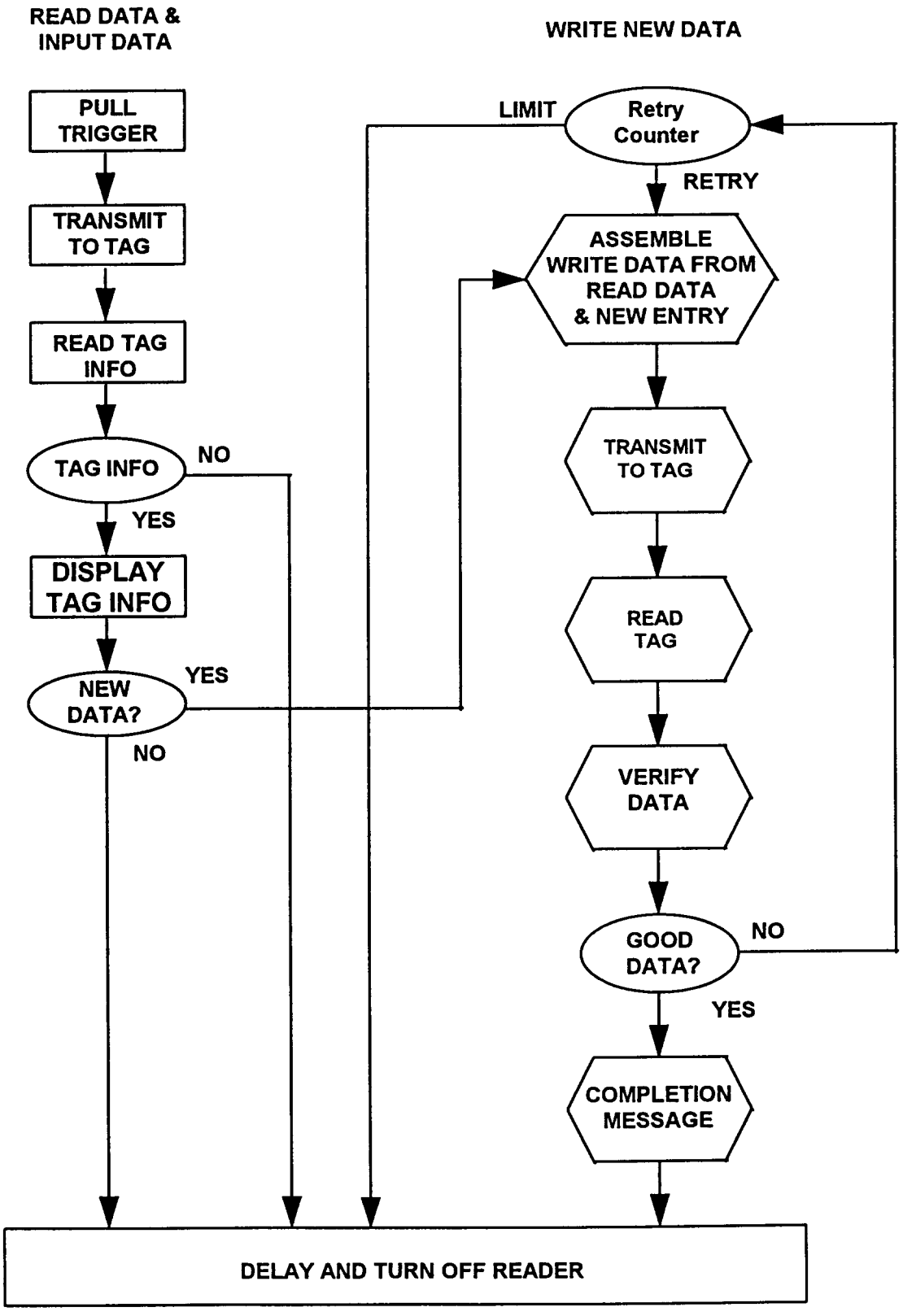
SYSTEM ARCHITECTURE
MRAM READ/WRITE TRANSPONDER



ATTACHMENT A

13 Jan 1995/emv

FUNCTIONAL FLOW CHART



ATTACHMENT B

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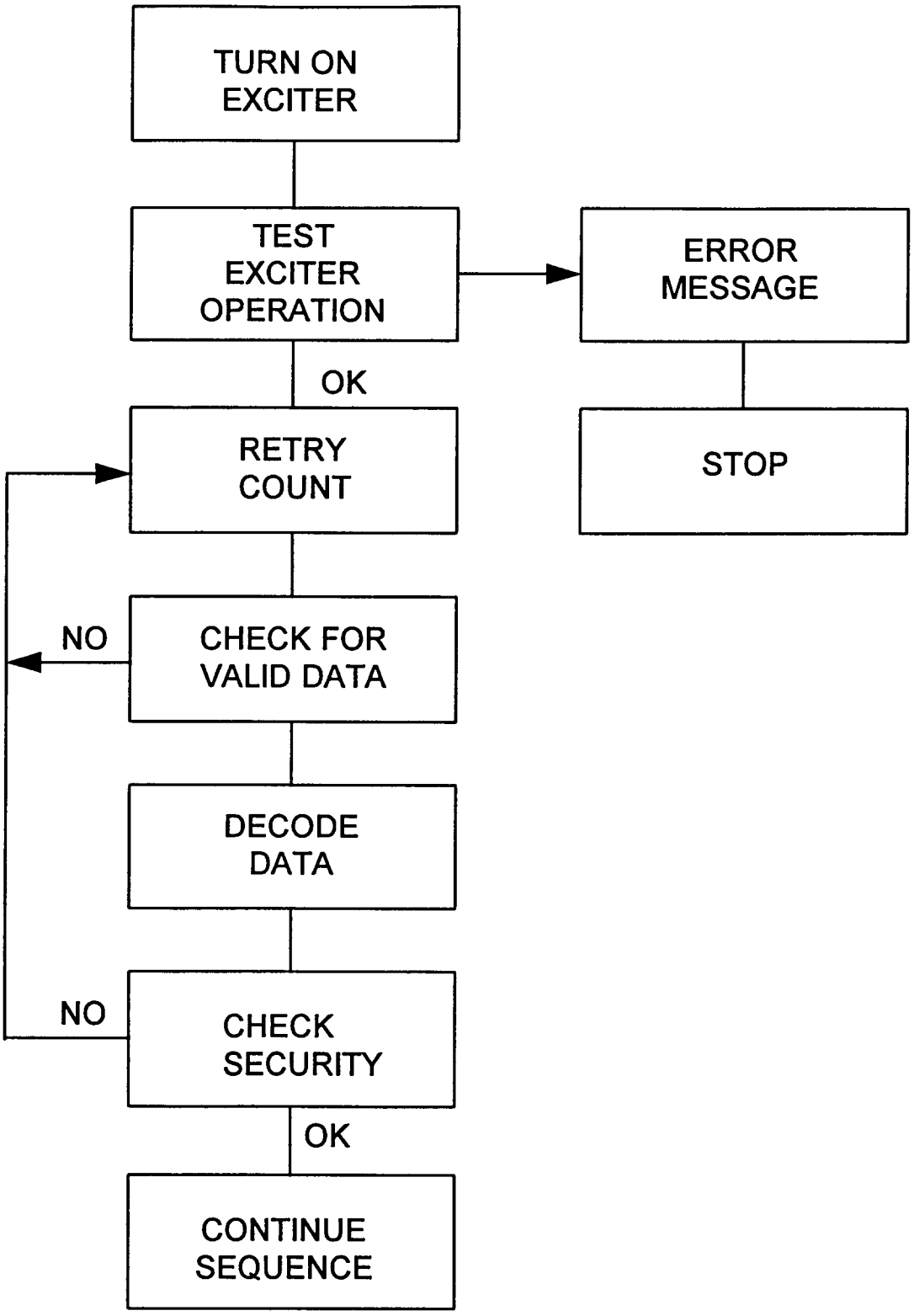
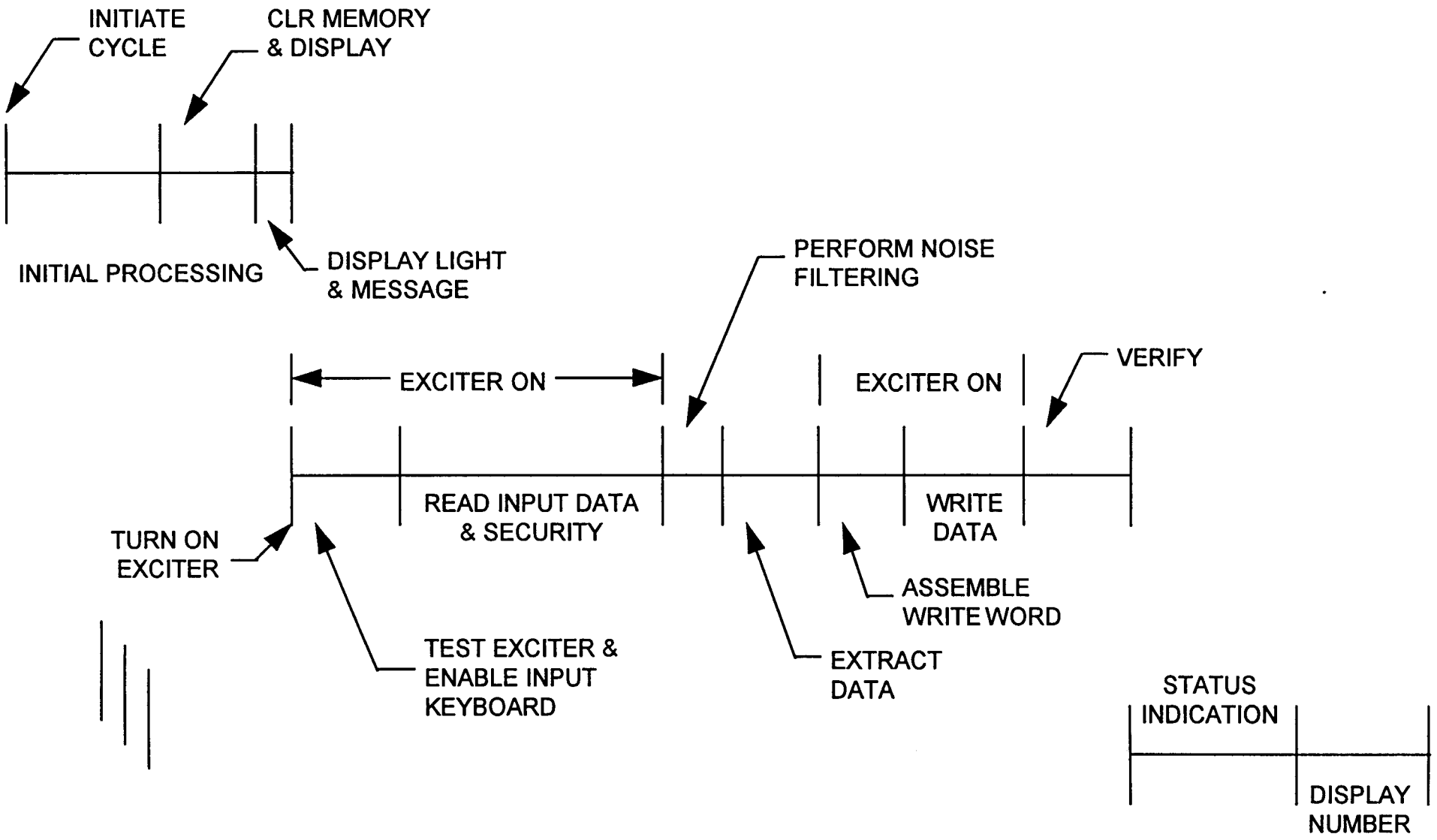
DATA READ SEQUENCE

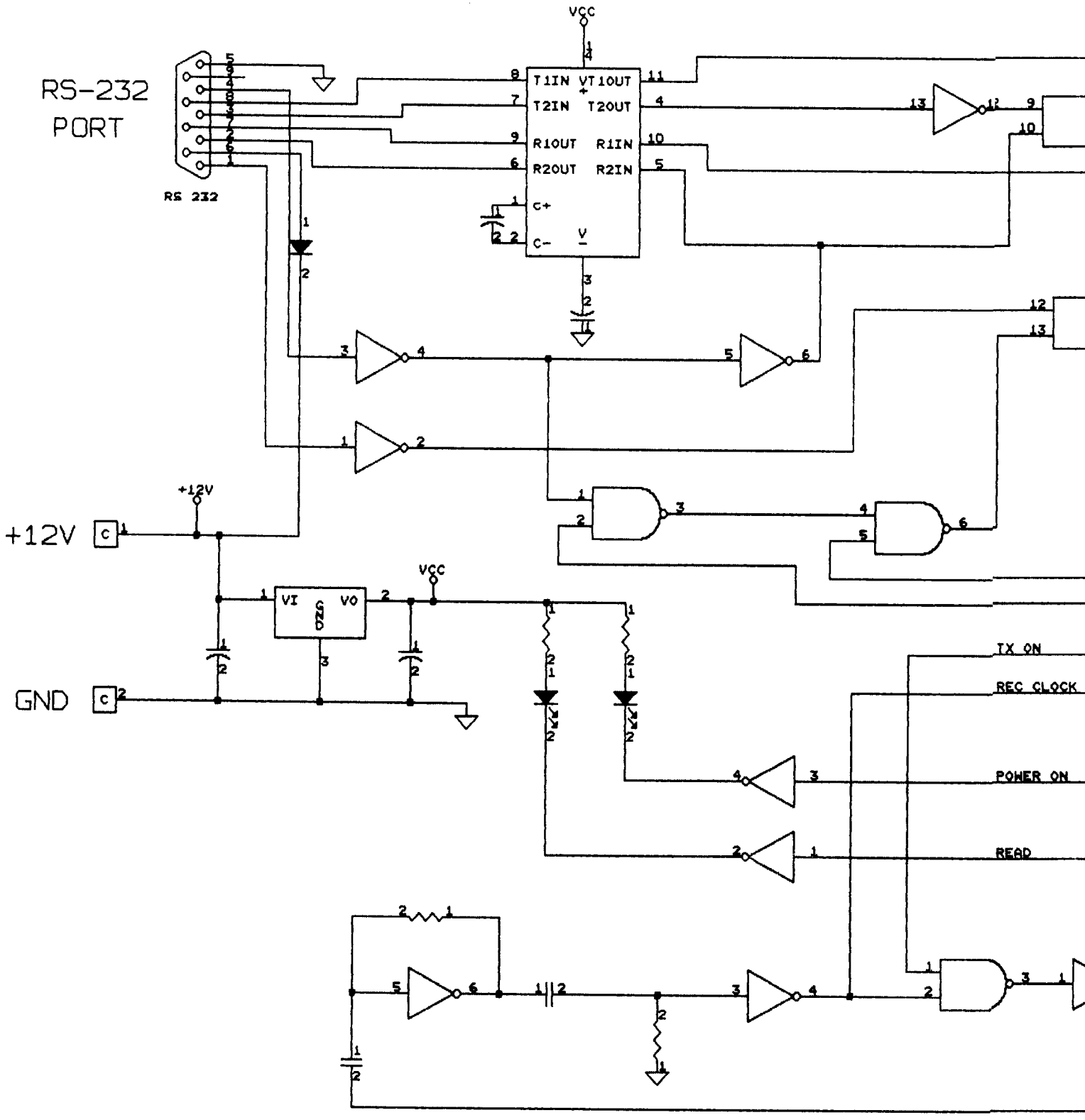


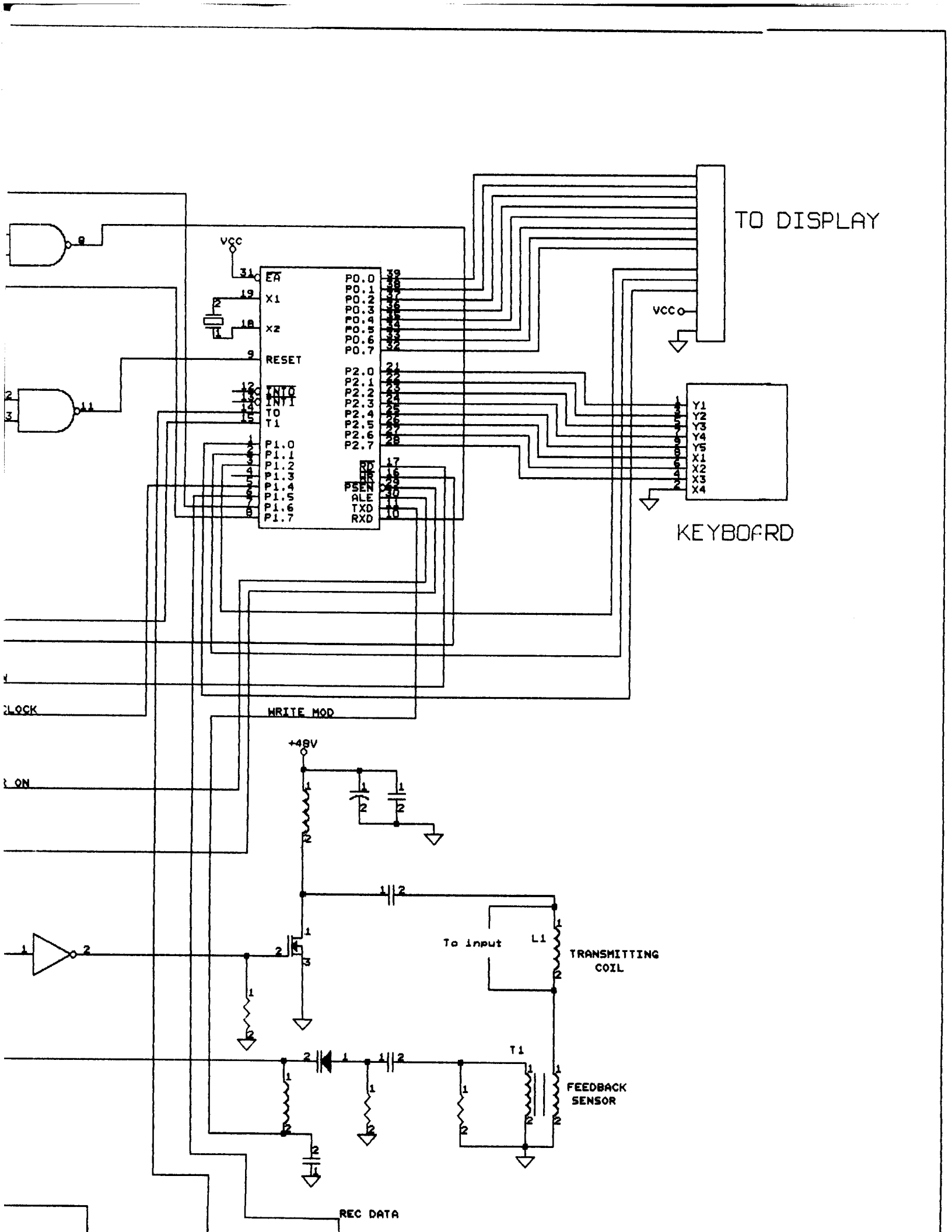
ATTACHMENT C

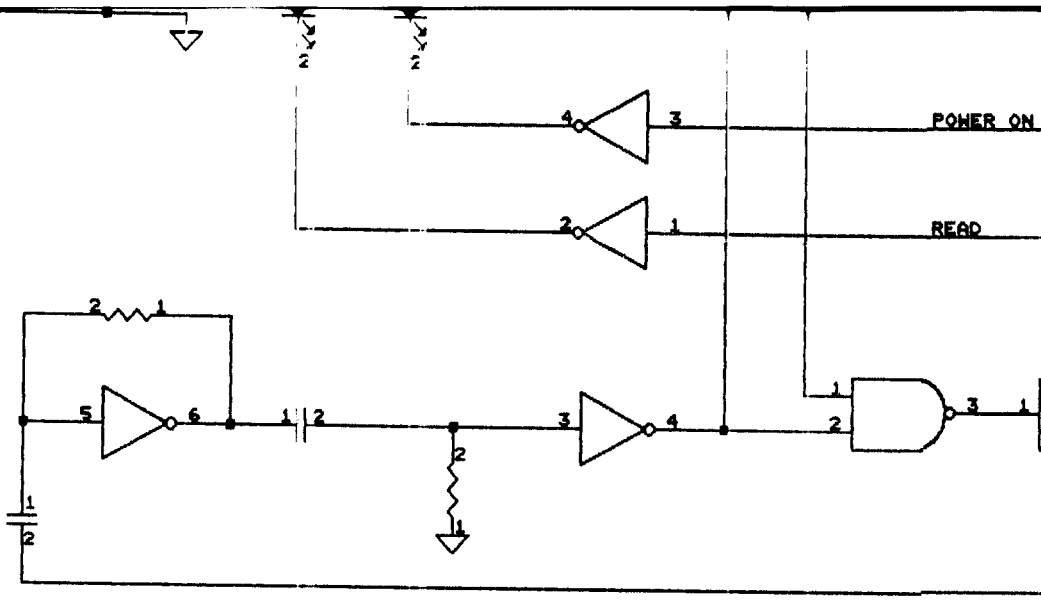
SUGGESTED READER/WRITER CYCLE TIMING

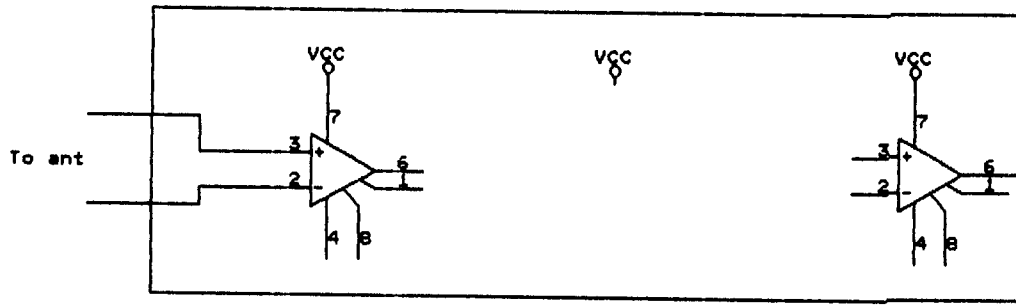


ATTACHMENT D

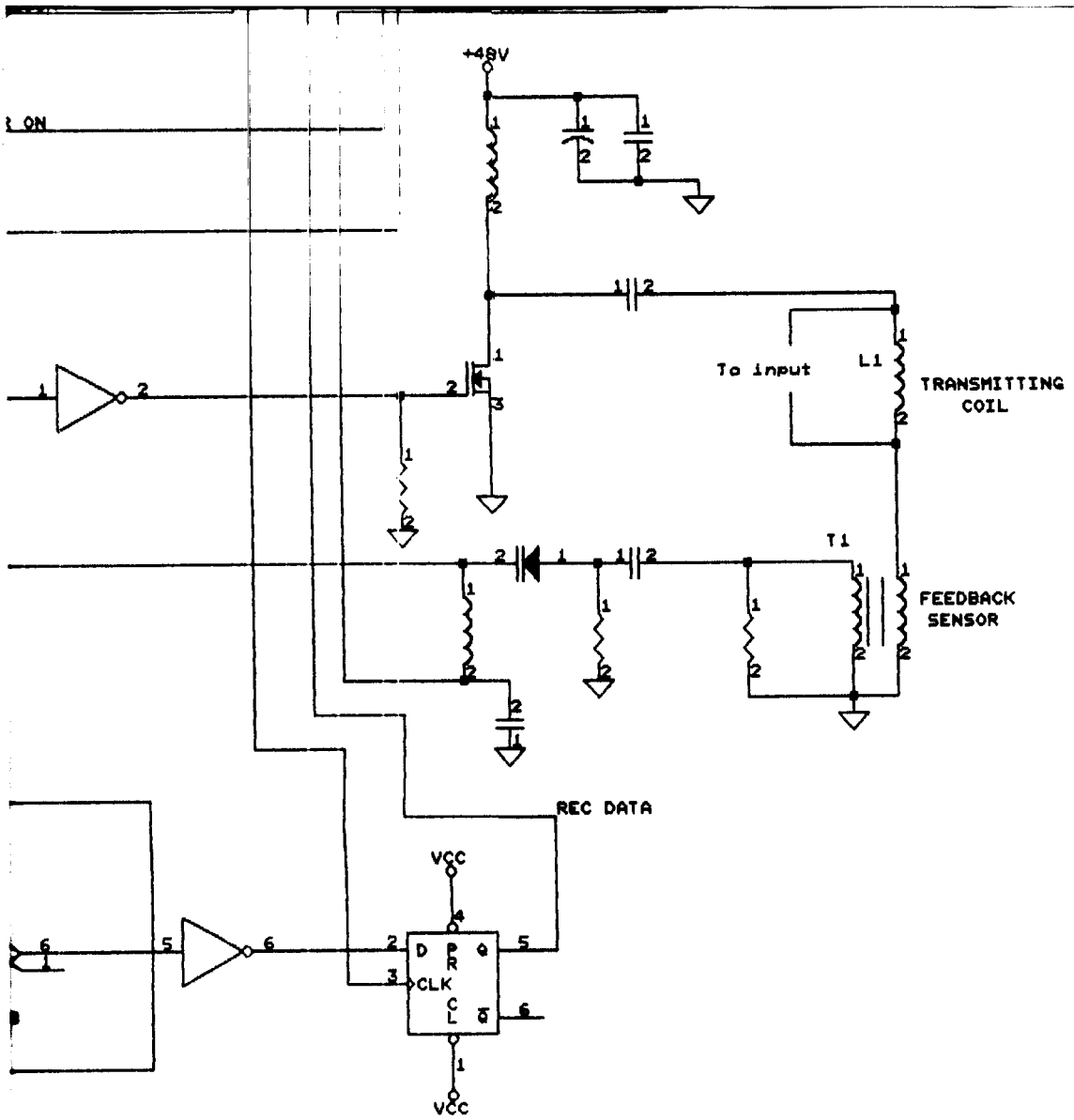

RS-232
PORT
RS 232
VCC
T1IN
T2IN
R1OUT
R2OUT
C+
C-
V-
T1OUT
T2OUT
R1IN
R2IN
+12V
GND
VI
VO
GND
IX ON
REC CLOCK
POWER ON
READ


TO DISPLAY
VCC
EA
X1
X2
RESET
INT0
INT1
T0
T1
P1.0
P1.1
P1.2
P1.3
P1.4
P1.5
P1.6
P1.7
P0.0
P0.1
P0.2
P0.3
P0.4
P0.5
P0.6
P0.7
P2.0
P2.1
P2.2
P2.3
P2.4
P2.5
P2.6
P2.7
RD
WR
PSEN
ALE
TXD
RXD
Y1
Y2
Y3
Y4
Y5
X1
X2
X3
X4
KEYBOARD
CLOCK
WRITE MOD
+48V
To input
L1
TRANSMITTING COIL
T1
FEEDBACK SENSOR
REC DATA





MULTISTAGE FILTER



W J SYSTEMS 415 W TRAVELERS TRAIL BURNSVILLE, MN. 55337 PROGRAMMER - READER	
Title	SCHEMATIC DIAGRAM
Size: C	Document Number:
Date: February 14, 1995	Sheet 1 of 1
	REV: A